Ph.D. Thesis

Stability of Polarization in Organic Ferroelectric Metal-Insulator-Semiconductor Structures

presented by

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'Almost everything you do will seem insignificant, but it is important that you do it'

Mahatma Gandhi

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Abstract

Organic thin film transistors (TFT) are an attractive option for low cost electronic applications and may be used for active matrix displays and for RFID applications. To extend the range of applications there is a need to develop and optimise the performance of non-volatile memory devices that are compatible with the solution-processing fabrication procedures used in plastic electronics. A possible candidate is an organic TFT incorporating the ferroelectric copolymer poly(vinylidenefluoride-trifluoroethylene) (P(VDF-TrFE)) as the gate insulator.

Dielectric measurements have been carried out on all-organic metal-insulator-semiconductor (MIS) structures with the ferroelectric polymer P(VDF-TrFE) as the gate insulator and poly(3-hexylthiophene) (P3HT) as p-type semiconductor. The capacitance spectra of MIS devices were measured under different biases, showing the effect of charge accumulation and depletion on the Maxwell-Wagner peak. The position and height of this peak clearly indicates the lack of stable depletion behavior and the decrease of mobility when increasing the depletion zone width, i.e. upon moving into the P3HT bulk.

The lack of stable depletion was further investigated with capacitance-voltage (C-V) measurements. When the structure was driven into depletion, C-V plots showed a positive flat-band voltage shift, arising from the change in polarization state of the ferroelectric insulator. When biased into accumulation, the polarization was reversed. It is shown that the two polarization states are stable i.e. no depolarization occurs below the coercive field. However, negative charge trapped at the semiconductor-insulator interface during the depletion cycle masks the negative shift in flat-band voltage expected during the sweep to accumulation voltages.

The measured output characteristics of the studied ferroelectric-field-effect transistors confirmed the results of the C-V plots. Furthermore, the results indicated a trapping of electrons at the positively charged surfaces of the ferroelectrically polarized P(VDF-TrFE) crystallites near the insulator/semiconductor interface during the first poling cycles. The study of the MIS structure by means of thermally stimulated current (TSC) revealed further evidence for the stability of the polarization under depletion voltages.

It was shown, that the lack of stable depletion behavior is caused by

the compensation of the orientational polarization by fixed electrons at the interface and not by the depolarization of the insulator, as proposed in several publications.[77,80,81] The above results suggest a performance improvement of non-volatile memory devices by the optimization of the interface.

Zusammenfassung

Organische Transistoren sind besonders geeignet für die Herstellung verschiedener preisgünstiger, elektronischer Anwendungen, wie zum Beispiel Radio-Frequenz-Identifikations-Anhänger (RFID). Für die Erweiterung dieser Anwendung ist es notwendig die Funktion von organischen Speicherelementen weiter zu verbessern. Das ferroelektrische Polymer Poly(vinylidenfluoride-Trifluoroethylen) (P(VDF-TrFE)) eignet sich besonders gut als remanent polarisierbarer Isolator in Dünnschicht-Speicherelementen.

Um Schalt- und Polarisationsverhalten solcher Speicherelemente zu untersuchen, wurden P(VDF-TrFE)-Kondensatoren und Metall-Halbleiter-Isolator-Proben sowie ferroelektrische Feld-Effekt-Transistoren (FeFET) aus dem Halbleiter Poly(3-Hexylthiophen) (P3HT) und P(VDF-TrFE) hergestellt und dielektrisch untersucht.

Die Charakterisierung der MIS-Strukturen mittels spannungsabhängiger Kapazitätsspektren machte deutlich, dass es nicht möglich ist, einen stabilen Verarmungzustand (Aus-Zustand) zu realisieren. Kapazität-Spannungs-Messungen (C-V) an MIS-Proben mit uni/bi-polaren Spannungszyklen zeigten eine stabile ferroelektrische Polarisation des P(VDF-TrFE)-Films. Eine Depolarisation des Isolators durch den Mangel an Minoritäts-Ladungsträgern[77,80,81] konnte als Grund für die Instabilität des Verarmungszustandes ausgeschlossen werden. Die C-V-Kurven wiesen vielmehr auf die Existenz fixierter, negativer Ladungsträger an der Grenzfläche hin.

Messungen von Output-Charakteristiken an FeFETs zeigten, dass diese fixierten Ladungsträger erst durch Anlegen einer äußeren Spannung an die Isolator/Halbleiter-Grenzfläche gelangen und nicht durch die Präparation. Die wahrscheinlichste Erklärung ist ein Elektronen-Transfer vom P3HT im Verarmungszustand, das heißt, beim Anlegen von positiver Spannung, an die Grenzfläche. Diese Ladungen werden an der Grenzfläche durch positive Polarisationsladung des P(VDF-TrFE) eingefangen (Charge Trapping) und energetisch und räumlich stabilisiert. Die Stabilität der Polarisation konnte durch die Untersuchung mittels thermisch stimulierter Ströme (TSC) bestätigt werden.

Zusammenfassend kann festgestellt werden: die Ursache der Ladungsträgerinstabilitäten in organischen ferroelektrischen Speicherelementen ist auf die Kompensation der ferroelektrischen Orientierungspolarisation durch "ge-

trappte" (fixierte) negative Ladungsträger zurückzuführen. Dieses Ergebnis liefert nun eine Grundlage für die Optimierung der Isolator/Halbleiter-Grenzfläche mit dem Ziel, die Zahl der Fallenzustände zu minimieren. Auf diesem Wege könnte die Stabilität des Speicherzustandes in organischen Dünnschichtspeicherelementen deutlich verbessert werden.

Contents

Acknowledgments **v**

Abstract **vii**

Zusammenfassung **ix**

1 Introduction **1**

2 Theoretical Background **7**
2.1 Morphology and Related Properties of the Materials 7
2.1.1 Poly(3-Hexylthiophene) 7
2.1.2 Polyvinylidene Fluoride and Its Copolymer 9
2.1.3 Current-Voltage Characteristics 12
2.2 MIS Capacitance Curves 14
2.2.1 Ideal Capacitance-Voltage Characteristics 14
2.2.2 Effect of Interface Charges on Current-Voltage Characteristics 18
2.2.3 Calculation of Semiconductor Interface Potential 22
2.2.4 Field-Effect-Transistor Equation 23

3 Preparation and Sample Characterization **27**
3.1 Device Preparation 27
3.1.1 Preparation of Poly(vinylidenefluoride-Trifluoroethylene) and Poly(3-Hexylthiophene) Solution 27
3.1.2 Preparation of Metal-Insulator-Metal (MIM) devices . . . 28
3.1.3 Preparation of Semiconductor Devices 31
3.2 Characterization Methods 34
3.2.1 Determination of Film Thickness 34
3.2.2 Impedance Measurements 35
3.2.3 Field-Effect Transistor Measurements 36
3.2.4 Thermally Stimulated Current Measurements 36
3.2.5 Current-Voltage Measurements 36
3.3 Fundamental Device Characterization 37

3.3.1 Characterization of Ultra-Thin Poly(vinylidenefluoride-Trifluoroethylene) Films 37
3.3.2 Lateral Current Inspection in Metal-Insulator-Semiconductor Structures 40

4 Ferroelectric Polarization in a Metal-Insulator-Semiconductor Device 47
4.1 Influence of Remanent Polarization of the Insulator on Maxwell-Wagner Effect at Semiconductor/Insulator interface. 47
4.2 Stability of Polarization in Organic Ferroelectric Metal-Insulator-Semiconductor Structures 55
4.3 Interface Traps at Semiconductor/Insulator interfaces 60
4.4 Effect of Stable Ferroelectric Polarization on the Field-Effect Transistor Performance 67
4.5 Effect of stable Ferroelectric Polarization on Thermally Stimulated Current (TSC) measurements 76

5 Final Conclusion and Outlook 85

Appendix 87
Modeling C-V Spectra 88
List of Symbols 93
Curriculum Vitae 95

Bibliography 99

Statement of Authorship/Selbstständigkeitserklärung 113

1 Introduction

Organic electronic devices, have been the focus of several studies in recent years,[2,30,62,68,80,81,124,125,131] and follow the same working principles as their inorganic predecessors. Classical inorganic electronics are based on the semiconducting properties of silicon and have been studied since the mid-20th century.[71,88,96,113] The combination of the semiconductor with an insulator creates a two layer structure, usually referred to as metal-insulator-semiconductor (MIS) or metal-oxide-semiconductor (MOS) device. Those devices are of great interest because they have the same structure as MOS field-effect transistors (MOSFETs or just FETs), which may be used in integrated circuits. The importance of FETs for electronic applications is based on the accumulation and depletion behavior at the semiconductor/insulator interface.

Large parts of the theory, initially developed for the evaluation of inorganic devices, appear to be still applicable to organic-based MIS structures, including organic field-effect transistors (OFETs).[2,68,81,125,131,133] Tsumura *et al.*[133] was one of the first to fabricate an organic FET based on polythiophene as the semiconductor and showed that the current-voltage characteristics are virtually identical to those of conventional inorganic FETs.

For the operation of organic as well as inorganic FETs, it is important to understand the physical processes related to the accumulation and depletion behavior, such as the charge mobility and charge trapping. The accumulation and depletion behavior can be well studied in MIS devices, which have, compared to the FET, a relatively simple design.[96,113] A transition from accumulation towards depletion is indicated by a decrease of capacitance vs. gate voltage (C-V). The position of the onset of this transition is referred to as the flat-band voltage or the threshold voltage and is defined by the zero field condition at the insulator-semiconductor interface. MIS devices are often used to study charge trapping effects at semiconductor interfaces.[88,96] For instance, a permanent change of charge density at the interface results in a shift of the flat-band voltage to either positive or negative values.[88] FETs, on the other hand, measure mainly lateral currents, i.e. lateral charge transport effects, which can be largely influenced by the dielectric and surface properties of the insulator.

In order to obtain OFETs for non-volatile memory applications, a fer-

roelectric gate insulator[48,77,79,80,102] has been incorporated into the field-effect transistor, which is in this case also referred to as ferroelectric field-effect transistor (FeFET). Poly(vinylidenefluoride-trifluoroethylene) (P(VDF-TrFE)) appears to be an ideal candidate for a remanently polarizable gate insulator. The working principle of these devices is to permanently change the charge density at the insulator/semiconductor interface by using a ferroelectric insulator, such as P(VDF-TrFE), which maintains its polarization. In this way the memory device can be kept either in the accumulation or depletion[102] mode, which defines the *on* and *off* states, respectively.

Indeed, P(VDF-TrFE) based FeFETs and MIS devices have been studied in combination with organic[71,77,124] as well as inorganic semiconductors[48,62]. Jung *et al.*[48] demonstrated, by using an additional gate electrode, that these kind of devices can be fabricated with an ultra thin P(VDF-TrFE) spincast film, which allows for gate-voltage operation well below 10V. The disadvantage of organic non-volatile memory devices, at the present stage of development, is caused by the relatively low mobility of the semiconductor. One limitation for the clock frequency at which memory devices and transistors can be operated is the mobility, which must be high enough to ensure a complete transfer of charge.[114] Sirringhaus *et al.*[111] and Cho *et al.*[15] have reported mobilities for poly(3-hexylthiophene) (P3HT) of ≈ 0.1 cm^2(sV)$^{-1}$ which is high for organic materials but still much lower than for inorganic semiconductors. Silicon for instance shows mobilities well above 100 cm^2(sV)$^{-1}$.[43] Hence, applications for high performance electronics, such as Notebooks etc., which require a high clock rate, are not in reach so far.

However, the advantage of organic materials is their processability.[22] Apart from the evaporation of electrodes, organic based electronics can be easily processed by spincoating or printing techniques. Furthermore, they can be placed on flexible substrates. This makes non-volatile data storage devices based on organic FeFETs especially attractive for low cost memory devices such as Radio-frequency identification (RFID) and smart tags. Promising switching characteristics and retention times for P(VDF-TrFE) based FeFETs have been published amongst others[55,108,109] by Gelinck *et al.*[35] as well as Naber *et al.*[79] They have reported switching times in the millisecond range as well as retention times of several hours, which led to a detoriation of currents in the *on* state and to a concomitant decrease of the *on*/*off* ratio by 30%. However, in order to obtain devices suitable for commercial applications, it is especially important to have long data retention times of months or maybe even years.

For the stability of the *on* and *off* state it is essential to have a trap-free semiconductor/insulator interface as well as a stable remanent polarization of the insulator. Nicollian and Goetzberger[96,116] (NG) distinguishes here between charges that are fixed at the insulator interface and those that are trapped in fast states (also known as interface traps, interface states or surface states).

The latter type of traps can be considered as energetically less deep than those associated with fixed charges.

Fixed charges reside at the interface and have to be compensated by the external voltage source leading to a a threshold voltage shift, i.e. instability. This threshold voltage shift may change, depending on the operation time and bias stress of the device. Singh *et al.*[109] demonstrated a strong shift of threshold voltage in the output characteristics of a FeFET with an increasing number of measurement cycles. This shift can eventually lead to a detoriation of the *on*/*off* ratio and limits the retention time of the memory device. In order to understand such instabilities and determine the nature of traps, organic semiconductors have been studied mainly in combination with several non-ferroelectric organics (such as polysilsesquioxane(PSQ) and polyimide (PI)), as well as inorganic (SiO_2) insulators. Threshold voltage shifts and the dynamics of charge trapping were further investigated by Salleo *et al.*[106] and Taylor *et al.*[124] However, other authors have also published on this issue for organic[54,148] as well as inorganic[141,142] devices.

Fast states (or interface traps) can exchange majority charge carriers with the semiconductor bulk. This process may be modulated by the applied probing voltage and, thus, identified by a stretch-out of the C-V plot and a concomitant peak in the loss-voltage characteristic.[96] Torres *et al.*[132] found threshold voltage instabilities for accumulation as well as depletion voltages caused by fast states at P3HT/PI interfaces. Similar results of hole trapping near the interface have been reported by Salleo *et al.*[106] who studied the organic semiconductor poly-9,9'dioctyl-fluorene-co-bithiophene (F8T2). Further studies on P3HT-based MIS devices were carried out by Alves *et al.*[2] using a method developed by NG to retrieve interface trap densities for majority charge carriers, i.e. holes.

The NG technique may yield good approximations of interface trap density, however, it probes only the interaction with the majority charge carriers. In order to develop organic ambipolar semiconductors, it is also important to understand and study the trapping of minority charge carriers. This type of charge carriers usually make only negligible contribution to the overall charge trapping process. Hence, the trapping process of minority charge carriers can not be studied with the NG method. Therefore, Taylor *et al.*[125] investigated the presence of electron traps at P3HT/PI interfaces by means of photo-excitation and with that made a contribution towards the development of n-channel and ambipolar transistors as well as organic photo transistors. Apart from the flat-band voltage instabilities, interface traps may also influence the charge transport behavior which is mainly confined to the interface region in FETs. Zen *et al.*[143] showed that the deposition of a hexamethyldisilazane (HMDS) monolayer onto the SiO_2 insulator may passivate hole traps leading to an increase of majority charge carrier mobility. Furthermore Chua *et al.*[18] demonstrated that the elimination of electron traps at the interface may result in n-type behavior

in organic semiconductors, which were thought to show only p-type activity.

The above discussed instabilities of the threshold voltage were mainly observed by trapping of either holes or electrons at the insulator/semiconductor interfaces in devices with a non-ferroelectric gate insulator. However, as already mentioned, non-volatile memory devices require a remanently polarizable gate insulator, such as P(VDF-TrFE). For these devices another source of instability was proposed by Naber *et al.*[76,79,80] They suggested that the lack of stable remanent depletion behavior of the studied P3HT/P(VDF-TrFE)-based MIS and FeFET devices is caused by the depolarization of the ferroelectric insulator at depletion voltages. They argued that the ferroelectric polarization of the insulator requires electrons at the insulator/semiconductor interface, which can not be supported by the p-type semiconductor P3HT. Hence, it was concluded, this lack of compensation charges would lead to the depolarization of the insulator. However, in the course of this work it will be clearly demonstrated, that the remanent polarization is stable in MIS devices in depletion mode.[50] Furthermore, it will be shown that enough electrons are permanently trapped (fixed) near the interface, to completely compensate (even slightly overcompensate) the ferroelectric polarization.

Naber *et al.* as well as Meijer *et al.*[68] have considered the presence of a small number of permanently trapped electrons at the semiconductor/insulator interface, but only for non-ferroelectric gate insulators. However, the scientific opinion of Naber *et al.* concerning fixed charges at ferroelectric P(VDF-TrFE) interfaces is ambiguous. They reject the idea that fixed charges might cause instabilities using the argument that charge injection into P(VDF-TrFE) 'is less probable because it is a wide band gap insulator'[79] on one side, but also acknowledge the possibility of entrapment[80] of electrons on the other side.

A very recent study by Nakajima *et al.*[84] about the switching dynamics of P(VDF-TrFE) layers in MIS devices based on α,ω-dihexylsexithiophene (DH-6T) has also produced evidence for a 'screening charge' situated at the semiconductor/insulator interface. Furthermore, Nakajima *et al.* suggest a lack of ferroelectric depolarization but gives no further statement about the stability of the ferroelectric polarization in the depletion regime. Rather, they consider the influences of the depolarization field[66] induced by the lack of compensation charges in the semiconductor under depletion.

A similar effect was discussed by Lim *et al.*[62] and Ma *et al.*[64] in terms of the introduction of a second dielectric layer as a additional blocking layer into a MIS device. Such a layer lowers the leakage current but constitutes another issue for the design of reliable memory devices. Since additional buffer layer may induce a depolarization field under short circuit condition or reduce the voltage drop over the active P(VDF-TrFE) layer when voltage is applied, these layers need to be further optimized as discussed, for instance, by Henkel *et al.*[40] Indeed, in organic based electronics, thin blocking layers were successfully

implemented for silicon oxide surfaces and lead to an enhancement of charge carrier mobility due to the reduction of trap sites at the interface.[18,146]

As mentioned above the work presented in this thesis yields strong evidence for the stability of the ferroelectric polarization of the P(VDF-TrFE) gate insulator in MIS devices and the presence of permanently fixed charges at the interface. Therefore, since a depolarization can no longer account for the observed lack of stable depletion mode in P3HT/P(VDF-TrFE)-based MIS devices, it appears necessary to modify the interface, to minimize the effect of charge entrapment. Further, it was shown, the insulator/semiconductor interface contains, in addition to the fixed electrons, also a density of hole traps, usually referred to as fast states.[116]

In this thesis P(VDF-TrFE) based MIS and FET structures have been studied by means of different dielectric characterizations, including capacitance spectra, TSC measurements, C-V and I-V characteristics of MIS devices as well as FET characteristics.

The thesis consists of three parts:

- chapter 2 is an introduction into the theoretical background including a short summary about morphology and important properties of P3HT and P(VDF-TrFE) and an introduction into the physics of MIS structures,
- chapter 3 provides details about the preparation and characterization of the insulator as well as MIS structures
- chapter 4 and 5 present the study of ferroelectric polarization by different dielectric measurements and the final conclusion, respectively.

For clarity, chapter 4 is further subdivided into five sections, each providing a more specific introduction into the individual field of research, the presentation of results and discussion as well as conclusions.

Section 4.1 presents a study of the all-organic MIS device with the ferroelectric P(VDF-TrFE) by means of capacitance spectra. Here, the spectra were measured under different biases, showing the effect of charge accumulation and depletion on the Maxwell-Wagner peak. The position and height of this peak shows clearly the lack of stable depletion behavior and the decrease of mobility when increasing the depletion-zone width, i.e. upon moving into the P3HT bulk.

In section 4.2 C-V and current-voltage (I-V) measurements have been carried out on all-organic MIS structures with the ferroelectric polymer P(VDF-TrFE) as the gate insulator. When the structure was driven into depletion, a positive flat-band voltage shift was observed arising from the change in polarization state of the ferroelectric insulator. When driven into accumulation,

the polarization was reversed. It is shown that the two polarization states are stable i.e. no depolarization occurs below the coercive field. However, negative charge trapped at the semiconductor-insulator interface during the depletion cycle masks the negative shift in flat-band voltage expected during the sweep to accumulation voltages.

Section 4.3 shows that by means of a unipolar/bipolar voltage pattern the influence of the ferroelectric switching on the C-V data of the MIS device can be removed and that the conductance method[96,113] can be applied to determine the interface trap density. Hence, it turns out, the P3HT/P(VDF-TrFE) interface contains both the structurally fixed positive charges (see section 4.2) and a distribution of fast traps sites for majority charge carriers, i.e. holes.

Section 4.4 presents the study of the output and transfer characteristics of FeFETs. The FeFET measurements confirm the previous results on the stability of the ferroelectric polarization and the presence of negative charges at the insulator/semiconductor interface. Furthermore, the output characteristics suggest the permanent trapping of negative charges at the interface during the first poling steps, leading to an increased drain current for negative drain voltages with increasing number of poling cycles.

In section 4.5 the MIS device is subjected to thermally-stimulated current (TSC) measurements. Here three relaxations at −35°C, 25°C and 50°C are measured. The first two are assigned to the glass transition and an interface polarisation effect at crystallite boundaries, respectively. This interface polarization presents further evidence for the stability of the polarization under depletion voltages. The exact origin of the relaxation above 50°C could not be inferred from this measurement. However, it might be related to the charge trapping at the semiconductor/insulator interface.

2 Theoretical Background

2.1 Morphology and Related Properties of the Materials

Sections 2.1.1 and 2.1.2 present an introduction into morphology and related properties of P3HT and P(VDF-TrFE), respectively. The conformation of the P3HT molecules strongly influence the electronic properties of the semiconducting layer. The crystalline modifications of PVDF and P(VDF-TrFE) are also important, since they have a significant effect on the ferroelectric properties of the spincoated film. Section 2.1.3 gives an introduction into the measurement of the ferroelectric polarization in P(VDF-TrFE) films by current-voltage characteristics.

2.1.1 Poly(3-Hexylthiophene)

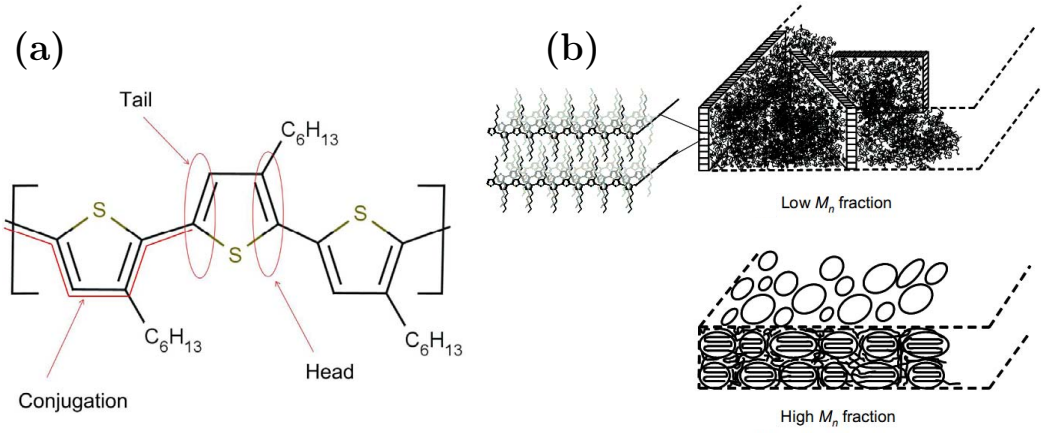

Figure 2.1: (a) Regio regular conformation of P3HT. The hexyl groups are arranged in a Head-to-Tail(HT) coupling. The position of the hexyl group marks the Head and the opposite side the Tail of the thiophene ring. (b) (Source: Zen *et al.*[145]) Morphology of P3HT for high and low molecular weight.

Structure and morphology of regioregular poly(3-hexyl thiophene) (rrP3-HT) is shown in Fig. 2.1(a) and (b). The π-bonds form the conjugated back-

bone of P3HT. The length of an unperturbated backbone is referred to as conjugation length. Since the π electrons are delocalised and may move along these conjugated backbones the conjugation is mainly responsible for the electronic and optical properties of rrP3HT.[9] The hexyl group, however, is isolating since it lacks delocalised electrons due to its σ-backbone. Nevertheless, the position of the hexyl group is important for the conjugation of P3HT, since it influences the selforganised arrangement of the P3HT chain as has been shown by Prosa *et al.*[101] and Bao *et al.*,[3] Siringhaus *et al.*[110,111] as well as others.[53] Self organisation of rrP3HT into a planar conformation makes it feasible to obtain relatively high mobilities in solution processed thin films.[3]

The position of the hexyl group marks the head of the thiophene ring and the opposite side its tail. The rrP3HT molecule assembles in Head-to-Tail(HT) coupling. That kind of arrangement of side chains allows P3HT to aggregate in highly ordered domains, which are embedded in to an amorphous matrix. In the disordered matrix, charge transport is mainly limited by hopping processes.[110] Zen *et al.*[146] have studied the aggregation as well as its effect on the hole mobility of P3HT for different molecular weights and developed morphology schemes for high and low molecular weights, given in Fig. 2.1(b).[20,65] He showed that the mobility increases with the molecular weight. Most of the crystalline domains in the low-molecular weight layers are isolated by the amorphous matrix, and transport will be mainly between the few interconnected domains. However, in the high molecular weight layers, a larger number of chains organizes in ordered domains and creates therewith many possible pathways for the carriers to travel.[145]

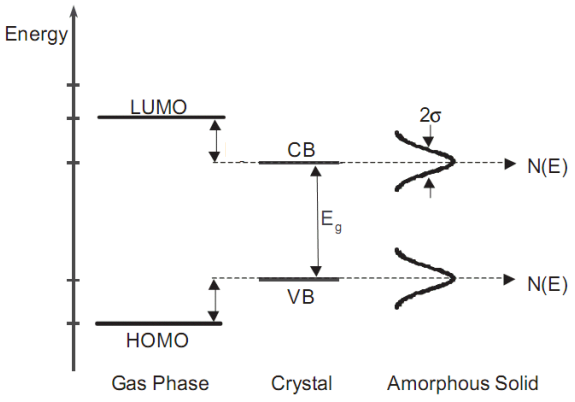

Figure 2.2: Energy levels of an isolated molecule, i.e. gas phase (left), a molecular crystal (middle) and an amorphous solid. The width 2σ of Gaussian distribution of localized states (density of states) $N(E)$ defines the the band width of the HOMO and LUMO level. (Source: 'Physics of Organic Semiconductors'[10])

The above mentioned π bonds in organic semiconductors, such as P3HT, give rise to energetic levels, i.e. molecular states: the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO), as illustrated in Fig. 2.2.[4,9,10,146] In unordered organic materials the sum off all these levels form a Gaussian distribution of localized states. This distribution of HOMO and LOMO levels can be, in analogy to inorganic semiconductors

physics, considered as valence and conduction bands. The charge transport is, unlike in inorganic semiconductors, rather incoherent and realized by hopping, i.e. Poole-Frenkel effect, from one state to another.[6,32] Hopping describes a thermally activated tunneling process between chains or chain segments, i.e. localized states, and is therefore less efficient as the coherent charge transport in crystalline structures.[5,6,32,41,99]

2.1.2 Polyvinylidene Fluoride and Its Copolymer

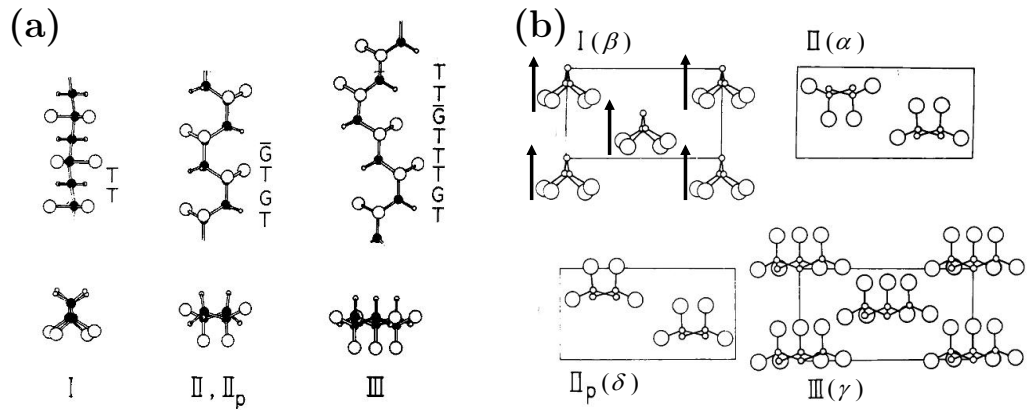

Figure 2.3: (Source: Tashiro *et al.*[121]) Molecular structure (a) and crystalline modification (b) of PVDF which are referred to as Form: I(β), II (α), II_p (δ) and III (γ). The arrows in (b) indicate the net dipole moment of the β-form.

Fig. 2.3(a) and (b) illustrates the four crystalline modifications of PVDF, referred to as form I (β), II (α), II_p (δ), which is the polar configuration of form II, and III (γ).[85] The α and δ PVDF have the same molecular conformation $\bar{G}TGT$ but differ in the chain arrangement. The unit cell of α and δ PVDF, as depicted in Fig. 2.3(b), consists of two chains, each with an associated dipole moment. In α PVDF the dipole moment of each chain is oriented into opposite direction with respect to its neighbors, thus, the net dipole moment is zero. The parallel orientation of the dipole moments yields the polar unit cell of δ PVDF. A non-zero net dipole moment is also associated to the γ PVDF, which requires a $TTTG\bar{T}TT\bar{G}$ molecular structure. Melt processed films consist predominantly of the non-polar α PVDF, since it constitutes the thermodynamically most stable conformation. In this type of conformation the molecules are folded many times and are, assembled in the form of lamellae, which may form circular structures (> 100 μm) know as spherulites.[63]

Most interesting, from a technical point of view, is the large net dipole moment associated to the β PVDF. Its crystal structure is built of parallel aligned molecules with an all-trans (TT) conformation. Each $(CH_2 - CF_2)_n$ repeat unit carries a vacuum dipole moment of $\mu = 7 \times 10^{-30}$ Cm induced by the negative fluorine ($\delta+$) and positive hydrogen atoms ($\delta-$) as depicted in

Fig 2.4(a). The summation of μ over one unit cell volume yields a theoretical polarization of 130 mCm^2.[33] Hence, the TT conformation is the reason for the large polarizations of β PVDF films and may be obtained by stretching[1] α-PVDF films. During the stretching the lamellae conformation of the α-phase becomes destroyed and the molecules reorient parallel to the drawing direction.

The copolymer P(VDF-TrFE) on the other side, may crystallize mainly in all trans β-phase right from melt or solution. A detailed discussion how the crystallization depends on TrFE content as well as preparation was given by Tashiro *et al.*[86,121,122] Due to the similarity in the size of hydrogen and fluorine atoms, VDF and TrFE units are randomly distributed along the molecular $(-CH_2-CF_2)_n-(CH_2-CHF)_m$-chain to form a random copolymer and cocrystallize into a single crystalline phase analogous to β PVDF (Fig. 2.4(a)).[33] The TrFE units induces small defects in the polymer chain, which lead to the spontaneous all-trans arrangement of the molecule. Since β-phase in P(VDF-TrFE) is formed spontaneously, it is possible to produce solution processed films with high degree of crystallinity well above 50% depending on the amount of chain ordering defects.[26,82] These crystalline domains are then embedded in a non-crystalline amorphous matrix. In contrast to pure PVDF, P(VDF-TrFE) shows a clear Curie temperature, which changes with the mol%-content of TrFE. PVDF, on the other side, does not show a clear Curie temperature, since the the ferroelectric phase melts below the hypothetical Curie point.[33]

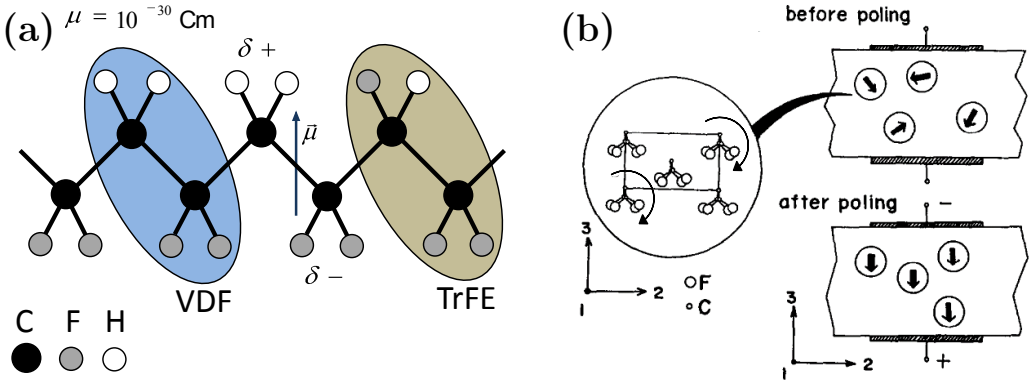

Figure 2.4: (a) Schematic of P(VDF-TrFE) molecule in the all trans β-phase. The arrow indicates the vacuum dipole moment of VDF repeat unit. (b) (Source: Tashiro *et al.*[122]) Illustration of the poling process in a crystal domain of P(VDF-TrFE). Arrows indicate the rotation of the molecules around their axis.

Degree of crystallinity of P(VDF-TrFE) as well as chain conformation may depend critically on the preparation details as well as the TrFE mol% content.[86,121,122] Typically three conformations have been reported, referred to

[1] Tamura *et al.*[120] for instance used PVDF films that were uniaxially stretched up to four times the original length at 65°C.

as high temperature (HT), cooled (CL) and low temperature (LT) phase (refer to Fig. 2.5). The non-ferroelectric HT phase is assumed to be a mixture of different gauge conformations (TG, $T\bar{G}$,$TTTG$ and $TTT\bar{G}$) and exists at elevated temperatures. When quickly cooled to room temperature the HT phase may result in CL phase, which consists of gauge and all trans conformations. The LT phase is essentially identical to form I of PVDF (TT) and may be obtained for instance by slow cooling from HT or CL phase, i.e. by annealing. Hence, both conformations, CL and LT, may be found in solution and melt processed films.[86] The 65 mol% VDF copolymer for instance is known to crystallize predominantly in LT phase with some fraction of CL phase.[123]

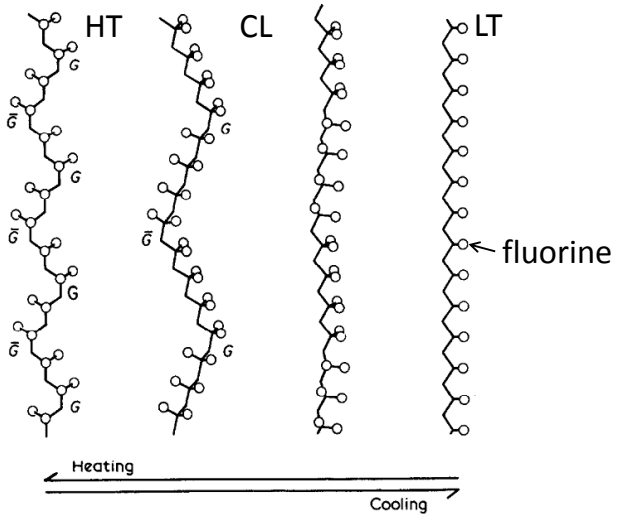

Figure 2.5: Illustration of molecular high temperature (HT), cooled (CL) and low temperature (LT) conformation of P(VDF-TrFE). The effect of ferroelectric phase transition is due to the large conformational change between the extended all-trans structure (LT) and the contracted chain structure with statistically disordered sequence of trans and gauche bonds (HT). (Source. Tashiro *et al.*[122])

The formation of crystalline β-PVDF gives rise to the ferroelectric polarization of P(VDF-TrFE) films of around 60 mC/m^2 with a coercive field of around 50 MV/m (refer to Fig. 3.7 on page 38).[33,77,136,138] This macroscopic effect of remanent polarization is attributed to the large net dipole moment of the β-conformation on one side and the fact that the molecular dipoles can maintain the orientation on the other side. When the coercive field is exceeded, the molecules start to rotate around their axis and align therewith their molecular dipoles along the field lines, as illustrated in Fig. 2.4(b).

The effect of stable polarization, however, is not only a pure intrinsic effect of P(VDF-TrFE) films but may be largely influenced by the presence of charges as discussed in reviews articles by Eberle *et al.*[26] and Eisenmenger *et al.*[28] Measurements presented in these articles suggest the depolarization of P(VDF-TrFE) films within minutes, when charge injection was prevented

by blocking electrodes. The remanent polarization and the coercive field may further be influenced when the thickness of the P(VDF-TrFE) film is decreased below 0.5 μm. Several authors[77,136–138] have shown that the decrease of film thickness leads also to a decrease of remanent polarization, however, increases the coercive field. This behavior is strongly amplified for film thicknesses below a critical thickness of around 0.15μm. The increase of coercive field and the decrease of remanent polarization is related to the increase of surface tension as well as the decrease of crystallinity in ultra thin films, respectively.[77,136–138]

2.1.3 Current-Voltage Characteristics

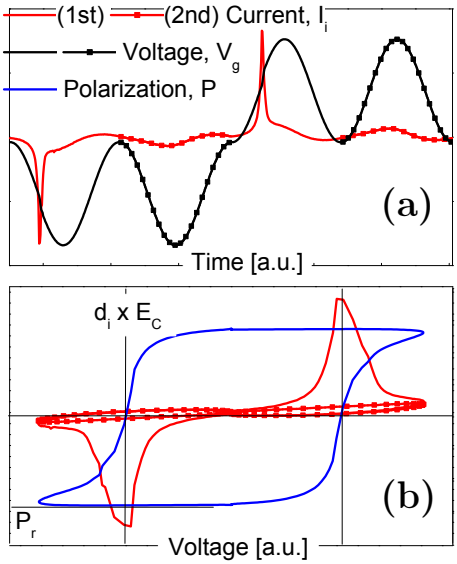

Figure 2.6: Example of the applied unipolar/bipolar voltage pattern and the corresponding current reading (a) of a ferroelectric insulator of thickness d_i as well as resulting Polarization P (b). Straight line and line with ■-symbols indicates the 1st and 2nd unipolar cycle, respectively.

Current-voltage (I-V) characteristics of ferroelectric insulators may contain contributions from the ferroelectric reorientation of the dipoles, pure capacitive effects and contributions from the ohmic conductance of the material. Bauer et al.,[7] Dickens *et al.*[21] but also other authors[66,135] have demonstrated the separation of these effects by means of a unipolar/bipolar voltage sweep method. For this method a voltage pattern $V_g(t)$, as exemplary shown in Fig. 2.6(a), is applied to the sample. The measured current $I_i = \mathrm{d}Q/\mathrm{d}t$ for an insulator with capacitance C and a ferroelectric polarization P and resistance R can be written as

$$I_i = C\frac{\mathrm{d}V_g}{\mathrm{d}t} + \frac{\mathrm{d}P}{\mathrm{d}t} + \frac{V_g}{R}. \tag{2.1}$$

The dielectric constant ε_r is related to C by $C = \varepsilon_0\varepsilon_r A/d$, which yields the pure capacitive contribution. The contribution of the polarization P to the measured current is $\mathrm{d}P/\mathrm{d}t$. The expression V_g/R represents the contribution of the ohmic resistance R.

A reversal of the ferroelectric polarization, when the coercive field is exceeded during an initial voltage sweep, will manifest itself as peak in the I-V plot. When a second unipolar sweep is undertaken, if P remains unchanged no current peak will be observed, in I_i, even though the coercive field is exceeded. Thus, if two unipolar voltage loops are applied to a ferroelectric only the current reading of the first contains a contribution of the switching of the ferroelectric dipoles.[21] Therefore, the pure polarization current I_p may be obtained by subtracting the current reading of the second loop I_2 from the first loop I_1 , i.e.

$$I_p = \underbrace{A\frac{\mathrm{d}P}{\mathrm{d}t} + C\frac{\mathrm{d}V}{\mathrm{d}t} + \frac{V}{R}}_{=I_1} - \underbrace{\left(C\frac{\mathrm{d}V}{\mathrm{d}t} + \frac{V}{R}\right)}_{=I_2}$$

$$I_p = A\frac{\mathrm{d}P}{\mathrm{d}t}. \tag{2.2}$$

Finally, the integration

$$P(t) = \frac{1}{A}\int_{t_0}^{t} I_p(t_m)\mathrm{d}t_m \tag{2.3}$$

yields the polarization. $P(t)$ can also be expressed as $P(V_g)$, since time and applied voltage V_g are measured simultaneously, i.e. V_g can be expressed as function of t. With knowledge about the film thickness d_i, V_g can of course also rewritten into the corresponding field $E = V_g/d_i$. For this type of measurement, the coercive field can not be measured directly and will, therefore, be defined by the position, that bisects the area of the polarization peak, i.e. $P_{max}/2 = P(E_c)$.[21] Hence, the polarization for the positive and negative voltages, as exemplified in Fig. 2.6(b), is given with $P(V_g) \pm P_{max}/2$.

2.2 MIS Capacitance Curves

2.2.1 Ideal Capacitance-Voltage Characteristics

In the following section the basic concepts of physics in MIS structures shall be recapitulated. Parts of the theory for inorganic MOS devices[89,117] appear still to be applicable to organic[81,124,126,131] electronics. A comprehensive discussion of the physics of inorganic MIS (or MOS) structures may be found for instance in *Physics of Semiconductor Devices.*[117]

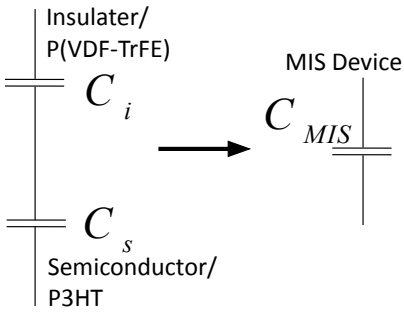

Figure 2.7: Equivalent circuit representing MIS device.

A common approach to describe and understand the capacitive behavior of MIS devices is a model based on an equivalent circuit. A simple representation of a MIS structure by such an equivalent circuit is obtained by the series combination of the capacitance representing the semiconductor C_s and the insulator C_i, as depicted in Fig. 2.7. The resulting capacitance of the MIS device is then expressed by

$$C_{\mathrm{MIS}} = \frac{C_i C_s}{C_i + C_s}. \tag{2.4}$$

Assuming a linear response of the insulator, its capacitance may be written as $C_i = \varepsilon_0 \varepsilon_i A/d_i$ with ε_0, ε_i, A and d_i as the permittivity of free space, dielectric constant, device area as well as insulator thickness, respectively. In the absence of mobile charge carriers the capacitance of the semiconducting layer may also be expressed in terms of its dielectric constant ε_s and film thickness d_s with $C_s = \varepsilon_0 \varepsilon_s A/d_s$. This expression however, is only valid for a fully depleted semiconductor or if charges, for what reason ever (blocking layer), can not be injected into the semiconductor. A complete description of C_s will be given below.

Using the continuity condition for the electrical displacement at the interfaces of the dielectrics the series combination of capacities yields[2]

$$\begin{aligned} \frac{1}{C_{\mathrm{MIS}}} &= \frac{1}{C_i} + \frac{1}{C_s} \\ \frac{V_{\mathrm{MIS}}}{Q_s} &= \frac{V_i}{Q_s} + \frac{V_s}{Q_s} \\ V_{\mathrm{MIS}} &= V_i + V_s \end{aligned} \tag{2.5}$$

[2]The electric capacitance C of a dielectric material is defined as ratio of charges at the dielectric surface Q to voltage V on the dielectric, $C = \frac{Q}{V}$.

with V_{MIS}, V_i, V_s and Q_s as the voltage drop over the MIS device, insulator, semiconductor as well as the number of charges at the semiconductor/insulator interface, respectively. The voltage drop over the semiconductor V_s is also referred to as band bending and is depicted in Fig. 2.8 for depletion (a) and accumulation (b).[38,90,117] Through an ohmic contact between electrode and

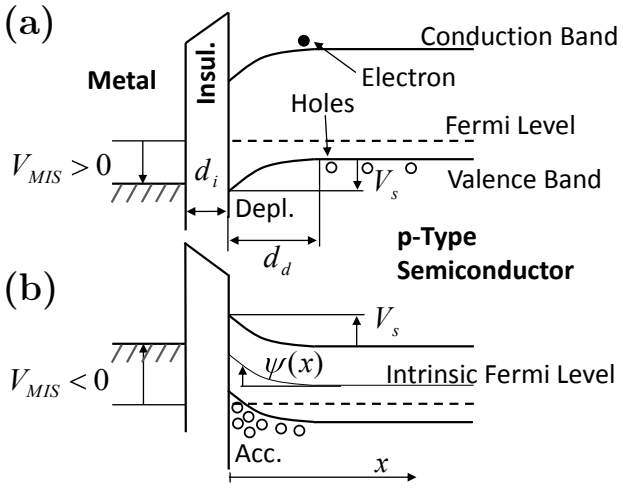

Figure 2.8: Band diagram of an ideal MIS structure at positive (a), i.e. depletion, voltage $V_{\mathrm{MIS}} > 0$ and negative, i.e. accumulation, voltage $V_{\mathrm{MIS}} < 0$. The band bending at the semiconductor interface leads in case (a) to a depletion zone of width d_d. A further depletion causes inversion and increase of number of electrons (minority charge carriers).

semiconductor (not depicted in Fig. 2.8) charges can be injected, which may then lead to accumulation or depletion of the semiconductor interface, for negative and positive gate voltages V_{MIS}, respectively. The depicted bending of the bands, described by $\psi(x)$, is a result of the total space charge distribution $\rho(x)$ in the semiconductor.[117] The total number of space charges, i.e space charge density $\sigma = Q_s/A$, with A as the device area, depends on $\psi(x = 0) \equiv V_s$. Solving the one dimensional Poisson equation[90,117]

$$\frac{\mathrm{d}\psi(x)}{\mathrm{d}x} = -\frac{\rho(x)}{\varepsilon_s} \tag{2.6}$$

for the surface potential at the semiconductor/insulator interface yields the space charge density

$$\sigma(V_s) = -\mathrm{Sign}(V_s)\sqrt{2}\left(\frac{\varepsilon_0\varepsilon_s}{\beta L_b}\right)\left[\underbrace{\left(e^{-\beta V_s} - \beta V_s - 1\right)}_{\text{majority charges}} + \underbrace{\left(\frac{n_i}{N_a}\right)\left(e^{\beta V_s} - \beta V_s - 1\right)}_{\text{minority charges}}\right]^{1/2} \tag{2.7}$$

with n_i, N_a, $L_b = \sqrt{\varepsilon_0\varepsilon_s/\beta q N_a}$ and $\beta = q/KT$ as intrinsic charge carrier concentration, doping density, Debye length and reciprocal thermal potential, respectively. The derived charge density $\sigma(V_s) = Q_s/A$, plotted in Fig. 2.9, yields a good description of the accumulation, depletion and inversion behavior of the semiconducting layer. Equ. 2.7 further be utilized to calculate capacitance of the semiconductor

$$C_s = \frac{\mathrm{d}Q_s}{\mathrm{d}V_s}. \tag{2.8}$$

This expression may now be used to calculate the capacitance of an ideal MIS system as it is measured with the probing signal $V_{sig}(t) = V_{\mathrm{MIS}} + V_{pr}\sin(\omega t)$. The term $V_{pr}\sin(\omega t)$ represents a small alternating voltage signal to probe the capacitative response of the MIS device, which is driven into either accumulation or depletion by the application of the semi-DC voltage signal, V_{MIS}. The general response of a MIS device as calculated by means of Equ. (2.4),(2.7) and (2.8) can be found in Fig. 2.9. Here, four regions may be distinguished: the

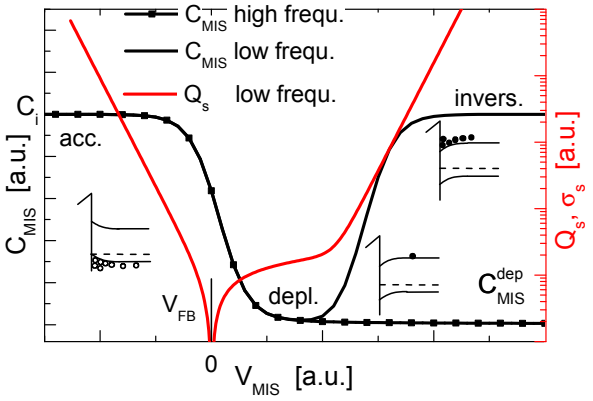

Figure 2.9: Schematic plot of C-V characteristics for a MIS structure as measured at high and low probing frequencies with corresponding variation of number of space charges, i.e. space charge density, in a p-type semiconductor, calculated with Equ. (2.7).[90,117] The band diagrams show the accumulation, inversion and depletion case.

accumulation, depletion, weak inversion and strong inversion. In accumulation, i.e. at negative voltages for a p-type semiconductor, the large number of charges within the semiconductor lead to $C_s \to \infty$ and consequently $C_{\mathrm{MIS}} \approx C_i$. An increase towards positive voltages yields a decrease of C_{MIS}, caused by the depletion and a concomitant decrease of the semiconductor capacitance, which is, in depletion, well approximated by $C_s = \varepsilon_0\varepsilon_s A/d_d$. The further increase of positive voltages may cause a inversion layer formation and hence an increase of minority charge carriers (electrons) leading finally to an increase of the MIS device capacitance towards $C_{\mathrm{MIS}} \approx C_i$. Such a behavior, however, is only measured at low probing frequencies, when generation-recombination rates of minority charge carriers and the charge exchange with the inversion layer can follow the probing signal.[117|3] At high measurement frequencies the minority charge carriers can no longer follow the signal, leading to a decrease of C_s and to the high frequency C-V characteristic also shown in Fig. 2.9. In deep depletion, the maximum depletion zone width is defined by the semiconductor thickness, i.e. $d_d = d_s$, yielding finally a MIS device capacitance of

$$C_{\mathrm{MIS}}^{dep} = \frac{A\varepsilon_o\varepsilon_i}{\varepsilon_i d_s + \varepsilon_s d_i}. \tag{2.9}$$

Such C-V characteristics are typically found for MIS devices, based on organic semiconductors.[37,80,84] The lack of inversion behavior, i.e. increase of capacitance, at depletion voltages is attributed to the lack of minority charge

[3]The response time for minority charge carriers in silicon at room temperature is typically 0.001s – 1s.[91]

carriers. A phenomenon probably caused by trap sites in the semiconductor near the interface. Chua *et al.*[18] have provided evidence that silanol groups at the SiO_2 gate dielectric interface in OFETs may be responsible for the trapping of electrons in several organic p-type semiconductors. Also polyimide (PI) insulators may lead to strong electron trapping near at the P3HT/PI interface as discussed by Taylor *et al.*[125] This charge trapping could be identified by its characteristic flat-band voltage shift, which will be further discussed in the next section 2.2.2. Hence, based on these results it may be concluded that electrons are likely to be present in most organic p-type semiconductors, however, basically immobile due to trapping.[125] Due to this trapping, electrons are unable to follow the ac probing signal and are also not available as inversion charges. The high frequency C-V characteristics as derived for inorganic MIS structures[90] reflects the lack of response of minority charge carriers, i.e. electrons, and yields therefore a valid description for the typically measured C-V characteristics of organic MIS structures.

To understand the working principle of a non-volatile memory device, the ferroelectric polarization behavior of the insulator has to be considered. A typical polarization curve of a P(VDF-TrFE) film is exemplified in Fig. 2.6. When introducing a ferroelectric insulator into the MIS stack, Equ. (2.5) has to be modified to account for the nonlinear behavior of the ferroelectric polarization $P(E_i)$ (in $[C/m^2]$) upon the field at the insulator E_i. Details about the derivation may be found in work of Miller *et al.*[71–73] or in the Appendix.

After modifying Equ. (2.5), V_{MIS} at the in MIS stack can be described with

$$V_{MIS} = V_s - \sigma(V_s)\frac{d_i}{\varepsilon_0\varepsilon_i} - P(E_i)\frac{d_1}{\varepsilon_0\varepsilon_i}. \tag{2.10}$$

Consequently, the field at the insulator is given by

$$E_i = -\frac{\sigma(V_s) + P(E_i)}{\varepsilon_0\varepsilon_i}. \tag{2.11}$$

Equ. (2.7), (2.10) and (2.11) yield a complete theoretical description of the capacitative behavior of the MIS structure and may be used to calculate the theoretical C-V characteristics (refer to Appendix). Although, such a numerical description will not be presented in this thesis, it is still worthwhile to consider Equ. (2.10) to gain an insight into the working principle of non-volatile memory devices. For this purpose it shall be assumed that, a positive or negative voltage was applied to the MIS system, large enough to exceed the coercive field E_c of the insulator into the corresponding direction. I this limit $P(E_i)$ becomes basically constant and can be replaced by the remanent polarization $P(E_i) = P_r = Q_p/A$. Hence, the polarization term in Equ. (2.10) can be simplified

$$P_r\frac{d_i}{\varepsilon_0\varepsilon_i} = \frac{Q_p}{C_i} = V_{FB} \tag{2.12}$$

with Q_p as number of remanent charges at the insulator interface, induced by the ferroelectric polarization of the insulator. In principle, Q_p may now act as fixed charge, influencing a shift of the threshold voltage, denoted as V_{FB}. Depending on the polarization direction, Q_p can be negative or positive and cause stable accumulation or depletion of the semiconductor, respectively (assuming a p-type). In other words, if the external voltage is removed, i.e. $V_{\mathrm{MIS}} = 0$ V, then V_{FB} constitutes an internal voltage source, influencing a field and with that a band bending at the semiconductor interface. Thus, once the coercive field has been exceeded, the molecular dipoles remain in their orientation and keep the device in accumulation or depletion. This effect may then be used in a FET configuration, where it causes a stable *on* or *off* state of the device. The phenomenon of threshold voltage shift, i.e trapped charges, on the C-V will be further considered in the following section.

It shall be mentioned again that the above consideration is only valid, once the coercive field has been exceeded and the polarization has been stabilized. The simplification becomes incorrect at the coercive field, i.e. when the polarization is changed. At this position, $P(E_c \approx E_i)$ strongly depends on the field and needs to be numerically evaluated.[71]

2.2.2 Effect of Interface Charges on Current-Voltage Characteristics

C-V characteristics not only provide information about the state of accumulation and depletion in the semiconductor layer, but also about the presence of interface charges, at the semiconductor/insulator interface.[96,127] In principle it is possible to discriminate between structurally fixed (or deeply-trapped) charges Q_f, which are immobile under an applied field and interface state charges Q_{it}, which strongly depend on V_s. The latter type of charge trap is also known as fast states or surface states,[116] which are energetically less deep than the structurally fixed charges.

The presence of fixed charges leads to band bending at $V_{\mathrm{MIS}} = 0$ and has to be compensated by an additional voltage to realize the flat-band condition. This additional bias causes a voltage shift of the ideal C-V characteristic, referred to as flat-band voltage shift

$$V_{\mathrm{FB}} = -\frac{Q_f}{C_i} + \underbrace{\phi_{ms}}_{=\phi_m - \phi_s} . \tag{2.13}$$

For the sake of completeness, Equ. (2.13) also contains a term representing the difference between the metal and semiconductor work functions, denoted as ϕ_m and ϕ_s, respectively. The band diagram of metal and semiconductor with its work functions before they come into contact is given in Fig. 2.10(a).

Fig. 2.10(b) shows the effect of positive and negative fixed interface charges on the C-V curve. At this point it shall be just mentioned that Q_f in principle is a net charge, which may consist of various type of charges having different physical properties such as polarity and electric field dependence.[4] In section 4.2 the idea of different type of charges will be adapted and further modified to model polarization charges of the P(VDF-TrFE) insulator as well as structurally fixed interface charges. This model about different charge types is also based on the considerations given at the end of the last section 2.2.1, were the effect of remanent polarization charge was discussed.

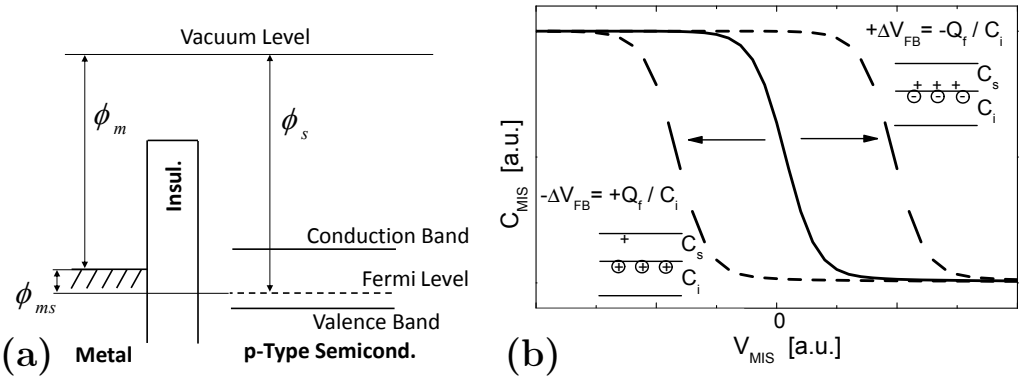

Figure 2.10: (a) Band diagram of metal and semiconductor before the contact making with semiconductor and metal work function, denoted as ϕ_s and ϕ_m, respectively. (b)Effect of structurally fixed charges $\pm Q_f$ on the C-V characteristics. Negative or positive charges cause shift of the flat-band foltage ΔV_{FB} towards positive or negative gate voltages V_{MIS}.

Interface traps (fast traps) are caused by defects located at the insulator/semiconductor interface and have, in contrast to the fixed charges, a strong field dependence (as discussed below).[2,36,92,126] Although developed for crystalline silicon, the model makes no appeal to any specific density of states distribution in the semiconductor, so that the approach is more general.[2] These states are energetically located between valence and conduction band and can exchange charges with the semiconductor bulk as illustrated in Fig. 2.11(a) for a p-type sample. In this process, interface states interact with the valence band by emitting or capturing holes. The occupancy of the filled states may now be modulated through the applied small ac field by moving the valence band, i.e. Fermi level, up and down. A change of the DC bias, on the other hand, leads to a (different) band bending and enables therewith the probing of the interface traps at different energetic cites.

This trapping process has its characteristic relaxation time[96] $\tau_{it} \propto \mathrm{Exp}(V_s -$

[4]The literature about inorganic MOS devices[116] discriminates for instance between oxide charges and ionic charges.

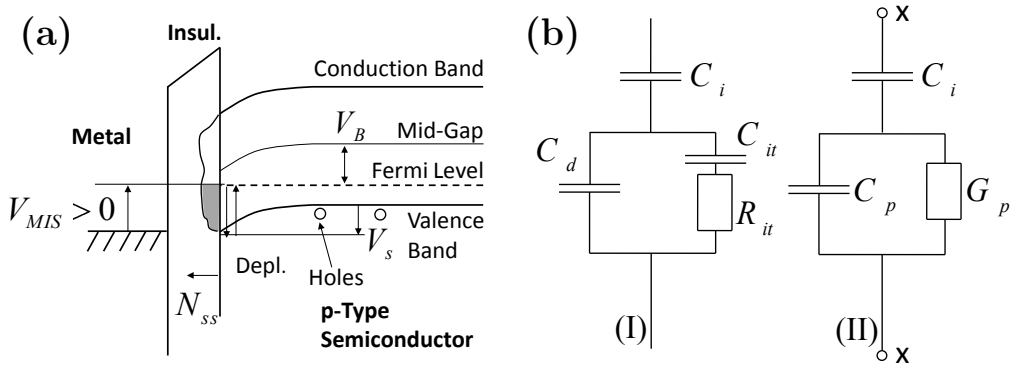

Figure 2.11: (a) Band bending of p-type semiconductor in depletion with arbitrary distribution of interface states N_{ss} at the semiconductor/insulator interface. (b) Equivalent circuit of a single interface trap level with relaxation time $\tau_{it} = R_{it}C_{it}$ (I) and its equivalent representation by a frequency dependent capacitance C_p and conductance G_p (II).

V_B),[5] which generally varies exponentially as function of the applied band banding V_s, i.e surface potential.[92,116] Due to τ_{it} the interface charges may not respond immediately to the applied ac signal, leading eventually to a loss peak in the spectra and the loss-voltage characteristics as illustrated in Fig. 2.12. The interface states lead also to a stretch out of the C-V curves. This is due to the fact that extra charges have to fill the traps. Hence, it takes more charges, i.e. applied voltage to obtain the same surface potential as for the case without interface states.

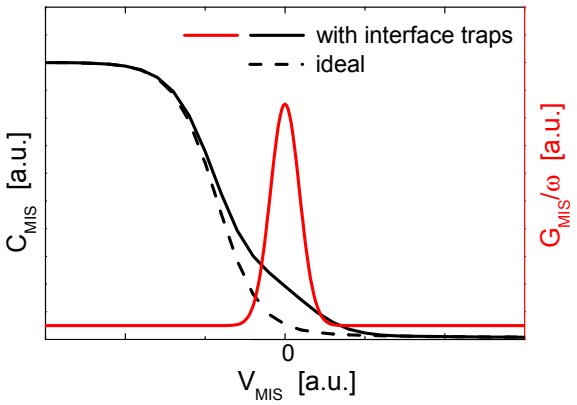

Figure 2.12: Effect of fast interface traps on the C-V, i.e. loss-voltage, characteristics. Interface traps cause trenching of C-V, in comparison to the ideal characteristics.

Interface traps may also be modeled by means of equivalent circuits. Fig. 2.11(b)(I) shows a relatively simple representation of a single level interface state with a single time constant. In this case, $\tau_{it} = R_{it}C_{it}$ is represented by a series branch of the majority carrier resistance R_{it} and interface state capacitance C_{it}. The insulator and depletion zone capacitance is given by C_i and

[5] V_B is the potential difference between the mid-gap and fermi level in the quasi neutral region of the semiconductor.

C_d, respectively. The parallel branch can be then translated into a frequency dependent capacitance C_p and conductance G_p as given in Fig. 2.11(b)(II), with[61,95]

$$C_p = C_d + \frac{C_{it}}{1+\omega^2\tau_{it}^2} \tag{2.14}$$

$$\frac{G_p}{\omega} = \frac{C_{it}\omega\tau_{it}}{1+\omega^2\tau_{it}^2}. \tag{2.15}$$

The height of the loss peak is governed by C_{it}, occurring at $\omega\tau_{it} = 1$. A relation between C_{it} and the interface trap density N_{ss} is obtained by using that $\mathrm{d}Q_{it} = qAN_{ss}\mathrm{d}E$ and $\mathrm{d}E = q\mathrm{d}V_s$. Hence, it follows that

$$C_{it} \equiv \frac{\mathrm{d}Q_{it}}{\mathrm{d}V_s}$$

$$C_{it} = Aq^2N_{ss}. \tag{2.16}$$

Equ. (2.16) and (2.14) may now be used to relate the loss peak maxium to N_{ss}, with

$$\left[\frac{G_p}{\omega}\right]_{max} = \frac{C_{it}}{2} = \frac{Aq^2N_{ss}}{2}. \tag{2.17}$$

The extraction of N_{ss} from $[G_p/\omega]_{max}$ is usually referred to as Conductance Method, a technique developed by Nicollian and Goetzberger.[96] In order to extract G_p/ω from the measured capacitance C_{MIS} and conductance G_{MIS} the insulator capacitance C_i has to be extracted. The admittance measured across the terminals x-x in Fig. 2.11(b)(II) is $G_{\mathrm{MIS}} + \mathbb{i}\omega G_{\mathrm{MIS}}$. Converting this to an impedance, subtracting the reactance of C_i, and converting back to an admittance, finally yiels[96]

$$\frac{G_p}{\omega} = \frac{\omega C_i^2 G_{\mathrm{MIS}}\left(G_{\mathrm{MIS}}^2 + \omega^2 C_{\mathrm{MIS}}\right)}{\omega^2 C_i^2 G_{\mathrm{MIS}}^2 + \left[\omega^2 C_{\mathrm{MIS}}\left(C_i - C_{\mathrm{MIS}}\right) - G_{\mathrm{MIS}}^2\right]} \tag{2.18}$$

$$C_p = \frac{C_i(G_{\mathrm{MIS}}^2 + \omega^2 C_{\mathrm{MIS}}^2)\left[\omega^2 C_{\mathrm{MIS}}(C_i - C_{\mathrm{MIS}}) - G_{\mathrm{MIS}}^2\right]}{\omega^2 C_i^2 G_{\mathrm{MIS}}^2 + \left[\omega^2 C_{\mathrm{MIS}}\left(C_i - C_{\mathrm{MIS}}\right) - G_{\mathrm{MIS}}^2\right]}. \tag{2.19}$$

This correction only requires knowledge about the actual value of C_i, which can be inferred from the C-V characteristics of the MIS device at accumulation voltages.

Although the approach with Equ. (2.14) only considers a single trap level, it conveys the concept of interface traps and their modeling. A more realistic description of the loss phenomenon is obtained by the introduction of a continuum of trap levels, represented by a network of R-C branches, which will be discussed in section 4.3.[6]

[6]The correction in Equ. (2.18) remains still applicable for a continuum of interface traps.

2.2.3 Calculation of Semiconductor Interface Potential

In section 4.3 fast interface traps are determined as function of the interface potential V_s. This quantity can not be measured directly but has to be inferred from the C-V characteristics. The surface potential $V_s(V_g)$ as function of applied gate voltage V_g can be calculated from the low-frequency capacitance $C_{lf} = \mathrm{d}Q_s/\mathrm{d}V_g$.[96] In this frequency regime the voltage drop across the insulator and semiconductor capacitance and its differential form is given by

$$V_g = V_s + \frac{Q_s}{C_i} \quad \text{and} \quad \mathrm{d}V_g = \mathrm{d}V_s + \frac{\mathrm{d}Q_s}{C_i}. \tag{2.20}$$

With $C_{lf} = \mathrm{d}Q_s/\mathrm{d}V_g$, integration of the rearranged equation (2.20) yields

$$V_s(V_g) = \int_{V_{\mathrm{FB}}}^{V_g} \left(1 - \frac{C_{lf}}{C_i}\right) \mathrm{d}V_g + V_s(V_{\mathrm{FB}}). \tag{2.21}$$

The integration constant $V_s(V_{\mathrm{FB}})$ has to be chosen in such a way that the band bending in the flat-band condition is zero. It would also be possible to determine the additive constant in the case of strong accumulation as described in detail by Nicollian and Goetzberger.[96]

It shall be mentioned that Equ. (2.21) constitutes an approximation, only valid for insulators with sufficiently high resistivity that is to say with $R_i \to \infty$. The increase of leakage current in ultra thin organic insulator films[48], however, may pose a problem for this kind of approximation. It is therefore worthwhile to consider the influence of a low R_i, in order to obtain a correct expression for $V_s(V_g)$ on one side and to retrieve a lower limit of R_i for which Equ (2.21) is true on the other side. In order to account for the insulator and semiconductor resistance the circuit in Fig. 2.7, on page 14, has to be modified as depicted in Fig. 2.13. Here, semiconductor and insulator resistance, denoted as R_s and R_i, respectively, are connected in parallel to semiconductor and insulator capacitance. A more general approach is, then, given by replacing the real with complex capacities, that is to say $C_i \to \tilde{C}_i$, $C_s \to \tilde{C}_s$ and $C_{lf} \to \tilde{C}_{lf}$. In a similar fashion to above, the series branch of these complex capacities $\tilde{C}_{lf}^{-1} = \tilde{C}_i^{-1} + \tilde{C}_s^{-1}$ yields

$$V_s(V_g) = \int_{V_{\mathrm{FB}}}^{V_g} \mathrm{Re}\left[1 - \frac{\tilde{C}_{lf}}{\tilde{C}_i}\right] \mathrm{d}V_g + V_s(V_{\mathrm{FB}}). \tag{2.22}$$

Here, it was used that only the real part $\mathrm{Re}[V_g/V_s] = \mathrm{Re}[1 + C_s/C_i]$ needs to be considered for the calculation of $V_s(V_g)$.

Since each complex capacity can be expressed as parallel branch of capacitance and resistance, as shown in Fig. 2.13, the integrand of Equ. (2.22)

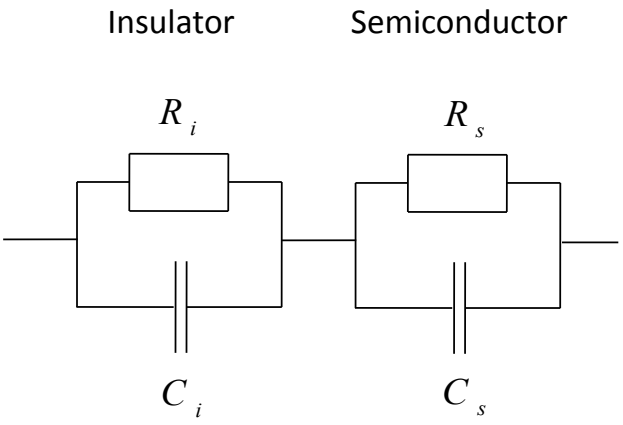

Figure 2.13: Equivalent circuit representation of a MIS structure (refer to Fig. 2.7, on page 14) with R_i and R_s as insulator and semiconductor resistance, respectively.

can be rewritten as

$$\mathrm{Re}\left[1 - \frac{\tilde{C}_{lf}}{\tilde{C}_i}\right] = \mathrm{Re}\left[1 - \frac{C_{lf} + (\mathbb{i}\omega R_{lf})^{-1}}{C_i + (\mathbb{i}\omega R_i)^{-1}}\right] \tag{2.23}$$

$$= 1 - \frac{\omega^4 C_i C_{lf} \left(R_{lf}\right)^2 R_i^2 + \omega^2 R_i R_{lf}}{\omega^4 C_i^2 \left(R_{lf}\right)^2 R_i^2 + \omega^2 \left(R_{lf}\right)^2}. \tag{2.24}$$

With the weak assumption that the overall resistance of the MIS device $R_{lf} = R_i + R_s$ will be largely governed by R_i, i.e. $R_i \approx R_{lf}$, we arrive at

$$\mathrm{Re}\left[1 - \frac{\tilde{C}_{lf}}{\tilde{C}_i}\right] = 1 - \frac{\omega^2 C_i C_{lf} + R_i^{-2}}{\omega^2 C_i^2 + R_i^{-2}}. \tag{2.25}$$

From this estimate it is possible to infer the lower limit for the insulator resistance. Hence, as long as $\omega^2 C_i C_{lf} > R_i^{-2}$, Equ. (2.21) yields a good approximation of the surface potential, since the capacity C_i is not shunted by the insulator resistance R_i.

2.2.4 Field-Effect-Transistor Equation

Fig. 2.14 shows a schematic illustration of a bottom gate FET as it was used for the measurements in section 4.4. When the forward bias is increased between source and gate charges become injected through the source and accumulate at the insulator/semiconductor interface (refer to section 2.2.1). This leads to formation of a conductive sheet near the interface, i.e. a channel, defined by channel width W and length L. Is a voltage applied between source and drain, this accumulation may then be monitored by means of the drain current I_D. This conduction process is described by hopping between neighboring localized states and is based on a Poole-Frenkel[5,6,32,41,99] effect.

An analytical expression for the drain current I_D can be found by using the differential expression for the field between source and drain, $\mathrm{d}V(x)/\mathrm{d}x$

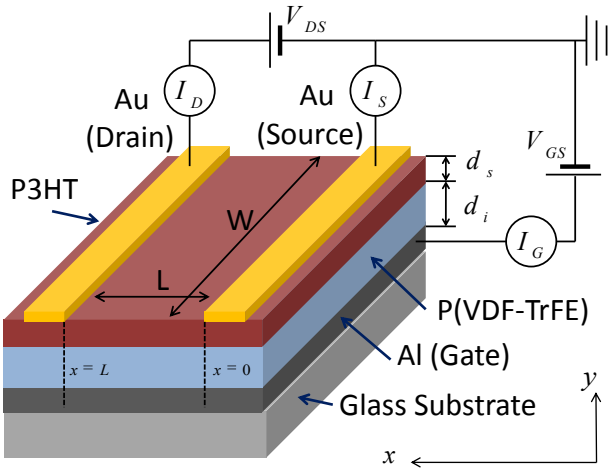

Figure 2.14: OFET layer structure with channel length (L = 100 μm), channel width (W = 14.85 cm) as well as the insulator and semiconductor thickness d_i = 0.3 μm and d_s = 0.06 μm, respectively. Measurement circuitry and the contact making is schematically depicted. The source contact is grounded.

with $x = 0$ at the source and $x = L$ at the drain contact. Thus the current density j_{DS} between source and drain may be written as

$$j_{\mathrm{DS}} = N_a(x) e \mu \frac{\mathrm{d}V(x)}{\mathrm{d}x} = \sigma \frac{\mathrm{d}V(x)}{\mathrm{d}x} \tag{2.26}$$

with $N_a(x)$, q, μ and σ as number density, elementary charge, drift mobility and conductivity respectively. For simplicity, N_a shall only depend on x and μ shall be considered as constant.[118] The charge at the interface can be expressed by

$$Q_s(x) = C_i \left[V_{\mathrm{GS}} - V_t - V(x) \right] = N_a(x) q W L d_s \tag{2.27}$$

where C_i, V_{GS} and V_t are the capacitance of the insulator, the voltage applied between gate and source as well as the threshold voltage (refer to section 2.2.2), respectively. Equ. (2.26) and (2.27) then yields the expression for the drain current $I_{\mathrm{DS}} = j_{\mathrm{DS}} W d_s$,

$$I_{\mathrm{DS}} = W C_i' \mu \left[V_{\mathrm{GS}} - V_t - V(x) \right] \frac{\mathrm{d}V(x)}{\mathrm{d}x} \quad \text{with} \quad C_i' = \frac{C_i}{WL}. \tag{2.28}$$

Separation of variables and integration from drain to source leads to

$$\begin{aligned} I_{\mathrm{DS}} \mathrm{d}x &= W C_i' \mu \left[V_{\mathrm{GS}} - V_t - V(x) \right] \mathrm{d}V \\ I_{\mathrm{DS}} \int_L^0 \mathrm{d}x &= \int_0^{V_{\mathrm{DS}}} W C_i' \mu \left[V_{\mathrm{GS}} - V_t - V(x) \right] \mathrm{d}V \\ I_{\mathrm{DS}} &= -\frac{W C_i' \mu}{L} \left[\left(V_{\mathrm{GS}} - V_t \right) V_{\mathrm{DS}} - \frac{V_{\mathrm{DS}}^2}{2} \right]. \end{aligned} \tag{2.29}$$

For the integration of the left hand side of the equation, Kirchhoff's law of charge conservation was used. The change of upper and lower limit of this integral reflects the current direction, which can be defined as positive or negative. The saturation regime is reached when the effective potential between

drain and gate becomes zero, i.e. $V_{DS} = V_{GS} - V_t$. In this voltage regime the injection of holes into the semiconductor is suppressed, leading to a flattening of the drain current. Hence, with the condition $V_{DS} = V_{GS} - V_t$, Equ. (2.29) simplifies to

$$I_{DS}^{s} = -\frac{WC_i'\mu}{2L}\left(V_{GS} - V_t\right)^2 \tag{2.30}$$

and can be conveniently used to calculate the mobility and the threshold voltage.

A reliable FET measurement requires a good insulating layer to ensure that $I_{DS} >> I_{GS}$, otherwise evaluation of the drain current becomes difficult. Under this condition, I_{DS} is independent from the gate current I_{GS} and may be measured as function of gate V_{GS} or drain voltage V_{DS} giving the transfer $I_D(V_{GS})$ or output $I_D(V_{DS})$ characteristic of a FeFET, respectively.[118,133]

3 Preparation and Sample Characterization

3.1 Device Preparation

The sections below provide detailed information concerning the preparation of the Metal-Insulator-Metal (MIM), Metal-insulator-Semiconductor, Semiconductor-Metal-Insulator-Metal (SMIM) devices as well as Field-Effect-Transistors.

3.1.1 Preparation of P(VDF-TrFE) and P3HT Solution

For the preparation of the poly(vinylidenefluoride-trifluoroethylene) (P(VDF-TrFE)) solution two solvents were used: Acetone with a purity of $\geq 99.7\%$ as well as 2-Butanone (MEK) with a purity of $\geq 99.5\%$ and a acetic acid content of $\leq 0.003\%$. The latter solvent was more suitable for thin film preparations below 1 μm, since P(VDF-TrFE)/2-butanone solution always produced smooth and transparent films. Further details about the P(VDF-TrFE) film preparation are given in section 3.1.2. The P3HT solutions were prepared with chloroform (purity 99%, stabilized with 1% ethanol.

All solutions were prepared in cleaned glass vials with teflon lids. It turned out that 2-butanone and chloroform can corrode the plastic of syringes and lids, which lead to pollution of the solution and consequently to speckles on the spincoated films. Therefore, it was necessary to use clean glass intead of plastic syringes in order to produce defect free, thin films. Syringes used for the preparation of poly(3-hexylthiophene) (P3HT) and P(VDF-TrFE) solution were always cleaned separately and never interchanged to avoid contaminations.

P3HT was purchased from American Dye Source, Inc. (ADS) with the following specifications:

- Molecular Weight (GPC): 60 000 g/mol (Polystyrene Standard)
- Polydispersity (M_w/M_n): 1.7

- UV-VIS (λ_{max}) Absorption: 446 nm
- Photoluminescence (λ_{max} Emission): 446 nm
- Metal content (Atomic Absorption analysis): Ni < 1 ppm

To promote the dissolution of the P3HT flakes the P3HT/chloroform solution was placed into an ultrasonic bath for about 1h. After that the solution was filtered twice, for precipitating possible unsolved particles. For the preparation of the organic electronic devices only one concentration of P3HT/solution was used (see Table 3.1)

The used copolymer, P(VDF-TrFE) (65/35 mol %), purchased from Solvey (Batch: 2P001), had the following specifications:

- Molecular Weight: $M_W = 1.97 \times 10^5$ g/mol (Polystyrene Standard)
- Melting Temperature: $T_M = 154,4$ °C
- Curie Temp.: $T_C = 106$ °C

In order to completely dissolve the P(VDF-TrFE) powder the solution was stirred at a temperature of 70°C for about 20 minutes. After the P(VDF-TrFE) was dissolved the preparation was finished with the filtering of the solution. Depending on the desired film thickness, different P(VDF-TrFE)/solvent concentrations were prepared ranging from 15 mg/ml up to 100 mg/ml. In Table 3.1 details can be found about the concentration and spin coating parameter for the respective layer thickness.

3.1.2 Preparation of Metal-Insulator-Metal (MIM) devices

The P(VDF-TrFE) capacitors (MIM devices), shown in Fig. 3.1(a) and (b) were prepared in an 3×3-array pattern (labeled as: 1A, 2A,...,1B,...1C,...). P(VDF-TrFE) capacitors as well as MIS and semiconductor-metal-insulator-metall (SMIM) devices, described below, were prepared onto cleaned glass substrates of size 1 mm × 24 mm × 24 mm. For cleaning the glass substrates were

1. manually rubbed with Deconex soap solution and subsequently rinsed with stain free water to remove all soap residuals,
2. placed into a soaking container filled with aceton and subjected to an ultrasonic bath for approximately 10 minutes (this step was afterwards repeated with isopropanol) and finally [1]

[1] If substrates needed to be stored for several days it turned out to be practicable to leave the samples in the isopropanol bath.

Final Film Thickness[μm]	**Solute/Solvent**	**Spincoating Parameter**
5	P(VDF-TrFE) / Acetone 100 mg/ml	1st 400 rpm (10 sec), 2nd 200 rpm (20 sec)
3.5	P(VDF-TrFE) / Acetone 100 mg/ml	1st 1000 rpm (10 sec), 2st 600 rpm (20 sec), 3rd 500 rpm (20 sec)
1	P(VDF-TrFE) / 2-Butanon 60 mg/ml	2000 rpm (10 sec)
0.5 (2 Layers)	P(VDF-TrFE) / 2-Butanon 30 mg/ml	1500 rpm (10 sec)
0.25	P(VDF-TrFE) / 2-Butanon 30 mg/ml	1500 rpm (10 sec)
0.25 (2 Layers)	P(VDF-TrFE) / 2-Butanon 25 mg/ml	1800 rpm (10 sec)
0.1 (2 Layers)	P(VDF-TrFE) / 2-Butanon 15 mg/ml	1000 rpm (10 sec)
0.05	P3HT / Chloroform 10 mg/ml	1500 rpm (10 sec)

Table 3.1: Parameters as used for the preparation of the P(VDF-TrFE) layer.

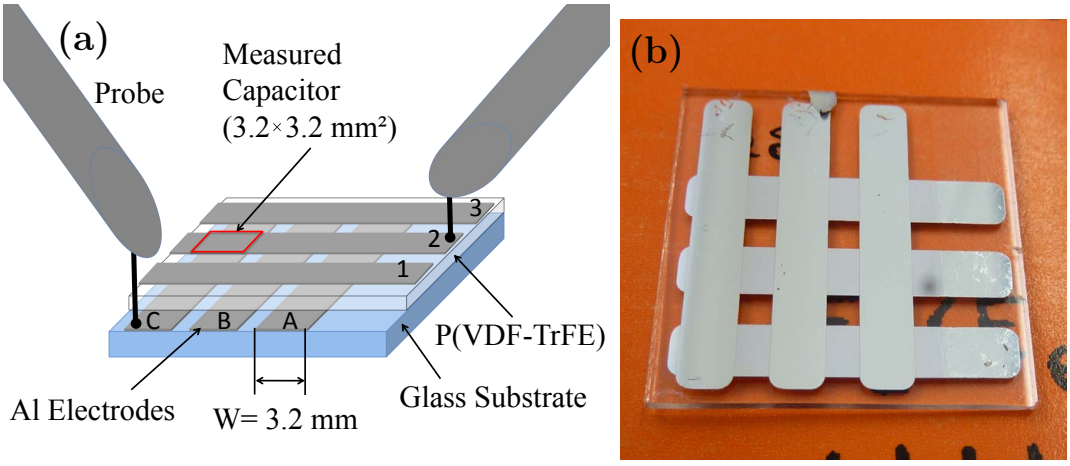

Figure 3.1: (a) MIM device consists of top Al electrodes (1,2,3) evaporated onto the P(VDF-TrFE) layer, which was spincoated onto a clean 1 mm thick glas substrate furnished with lower Al electrodes (A, B, C). In total 3×3 capacitors can be probed individually by contacting the corresponding electrodes. Contact making of capacitor $C2$ is shown exemplary. (b) Photograph of MIM device with a 0.5 μm thick (PVDF-TrFE) double layer.

3. dried with the nitrogen or heat gun.

Right after the drying the substrates were put into a closed plastic box to prevent further contamination with dust. Usually the cleaning was performed shortly before the evaporation of the 60 nm thick aluminium bottom electrodes.

After evaporation of the electrodes (trough a shadow mask) the P(VDF-TrFE) solution was spin coated onto the glass substrate (see Table 3.1 for more details) and placed onto a heating plate (110°C) until all samples of the batch have been spincoated. The spincoating was followed by a drying process under vacuum at 110°C for 12h in order to promote crystallization and further evaporation of residual solvents.[17,59,60,77,104,136] Concerning the annealing temperature, Xia *et al.*[136] and Naber *et al.*[77] have shown that annealing above 140°C may lead to a decrease of remanent polarization in thin films. This phenomenon occurs in thin P(VDF-TrFE) films only and is attributed to the reduction of the crystal size for low annealing temperatures below 140°C.[136] Xia *et al.* also pointed out that the use of a moderate annealing temperature leads to decreased switching times of the ferroelectric domains.

In the course of preparation, it was found that the spincoating of P(VDF-TrFE) double layer decreases the number of defects and thus increases the reliability of the insulator under bias stress. In this case the first layer was subjected to an intermediate drying step (under vaccum) for at least 4h at 110°C before the second layer was spin coated onto it. The surface quality of the film was independent from the used solute/solvent concentration. Crucial however is the spin coating procedure. The solution droplet should cover most of the substrate and the spin coating process has to start right after the application of the droplet. A delay of just seconds may result in the gradual evaporation of solvent at the edges of the droplet and produce stain as well as irregularities in film thickness. The preparation was concluded with the evaporation of the aluminum top electrodes.[2] The thicknesses of the films were measured on reference samples with a surface profiler *Dektak*^{3}*ST*. Finally, before the measurement could be started, the lower 'electrode-ends' of the bottom electrodes were cleaned carefully with aceton.

Concerning the solvent, it was found that the P(VDF-TrFE) solutions prepared with aceton produced poorer films compared to those prepared with 2-butanon. AFM images of P(VDF-TrFE) films spincoated from aceton and 2-butanon solution onto glass substrates with evaporated Al layers can be found in Fig. 3.2(a) and (b), respectively. The roughness of the aceton films was about 300 nm. The AFM picture clearly shows a rather porous surface, which

[2]Furthermore, it shall be mentioned that for some devices with film thicknesses > 1 μm also gold, deposited by sputtering, was successfully used as electrode material. However, for film thicknesses < 1 μm the sputtering of gold electrodes produced solely devices with short circuited top and bottom electrodes. This effect could be assigned to the deposition method, since devices with *evaporated* gold electrodes turned out to be stable under bias stress.

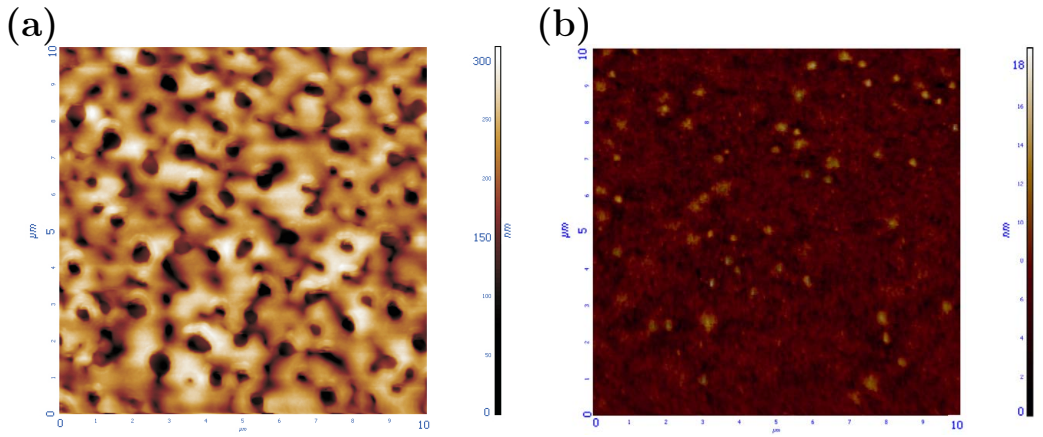

Figure 3.2: AFM picture (as produced by the AFM software) of 1 μm films spin coated from (a) P(VDF-TrFE)/aceton (b) P(VDF-TrFE)/2-butanone solution onto a clean glass substrate. Pictures show section of 10 μm $\times$ 10 μm. Some of the picture labels were resized for better readability. Picture (a) reveals a rough film with high amount of holes (roughness: $\approx$ 300 nm) whereas (b) shows a smooth surface with only a few small tippings (roughness: $<$ 18 nm).

is likely to be the reason for the cloudy appearance of the spin coated film. The holes or porosities also explain the breakdown of such films for thicknesses below $<$ 1 μm.

The 2-butanon film in Fig. 3.2(b) showed a relatively low roughness of $<$ 18 nm. Those films were basically defect (pin hole) free and had a transparent appearance (as can be seen in Fig. 3.1(b)). The tippings (or pinnacles), represented as white spots on the AFM picture did not cause any obvious electrical breakdown problems at elevated DC voltages. It is, however, worthwhile to focus on ways to prevent the formation of such tippings, in future studies, since they might have a negative effect on the charge mobility of thin film transistor (TFT) devices. It also transpired that a content of acetic acid above 0.003% in 2-butanone can lead to an increased film roughness comparable to roughnesses obtained with P(VDF-TrFE)/acetone solution.

3.1.3 Preparation of Semiconductor Devices

The MIS and Semiconductor-Metal-Insulator-Metal (SMIM) devices, schematically depicted in Fig. 3.3, were prepared in a microfabrication clean room[3] by sequentially spin coating two layers of P(VDF-TrFE) (65/35 mol %) from a 2-butanone solution onto a clean glass substrate furnished with evaporated Al electrodes.

Before the spincoating of the second layer the first layer was submitted

[3]Preparation of MIS and SMIM structures have been performed at the Bangor University, at the School of Electronic Engineering (Class 1000). Some MIS devices were also prepared at the Fraunhofer Institute in Potdam-Golm (Class 10000).

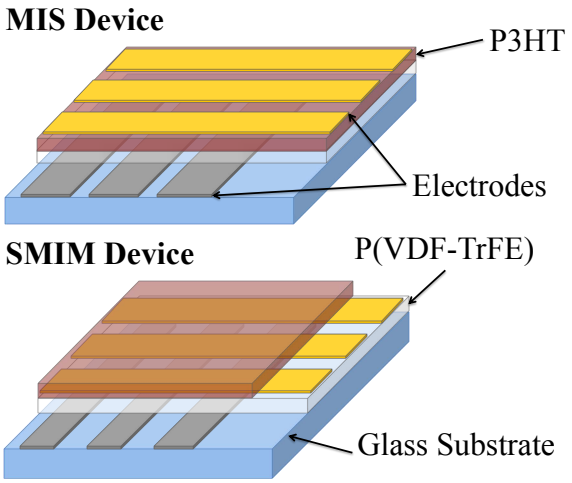

Figure 3.3: Schematic depiction of MIS (TOP) and SMIM (BOTTOM) device. Both kind of devices have similar electrode geometries.

to a intermediate drying step at 100°C for about 4h. Typical insulator layer thicknesses were 0.3 μm and 0.5 μm. After the second spincoating step the samples were submitted to a drying process under vacuum at 120°C for 12h.

In order to prepare MIS devices the p-type semiconductor P3HT, with a thickness of 0.05 μm, was spincoated, followed by the evaporation of the Au electrodes. For the SMIM structure the last two steps were inverted, i.e. the Au electrodes were evaporated before the spincoating of the P3HT layer. The preparation of the MIS and SMIM structures was concluded with a second annealing process under vacuum at 90°C for 10h.[143,144] Both kinds of devices, due to the top and the bottom electrode, define a square shaped capacitor with an area of 3.2×3.2 mm^2. Hence, the electrode geometry is the same as for the MIM devices, described above. Fig. 3.4(a) shows a photograph of a MIS device with Al/gold (bottom/top) electrodes, 0.3 μm thick P(VDF-TrFE) and 0.05 μm P3HT layer. The P3HT/P(VDF-TrFE) film was removed with acetone to uncover the contact area of the lower contacts (on the right-hand side). In order to obtain reliable contacts to the measurement probes, dots of silver paint were applied.

One batch of MIS devices were also prepared with patterned indium tin oxide (ITO) bottom electrodes. For the preparation of those devices a 25×25 mm^2 glass substrate with a pre-applied ITO layer was subjected to an etching procedure in order to obtain a finger (or stripe) like electrode geometry, comparable to the evaporated Al electrodes. Before and after the etching the samples were cleaned with

1. acetone,
2. Deconex soap solution and
3. iso-propanol.

For each of these cleaning steps the samples were placed in a soaking container and subjected to an ultrasonic bath for approximately 10 minutes. The finger

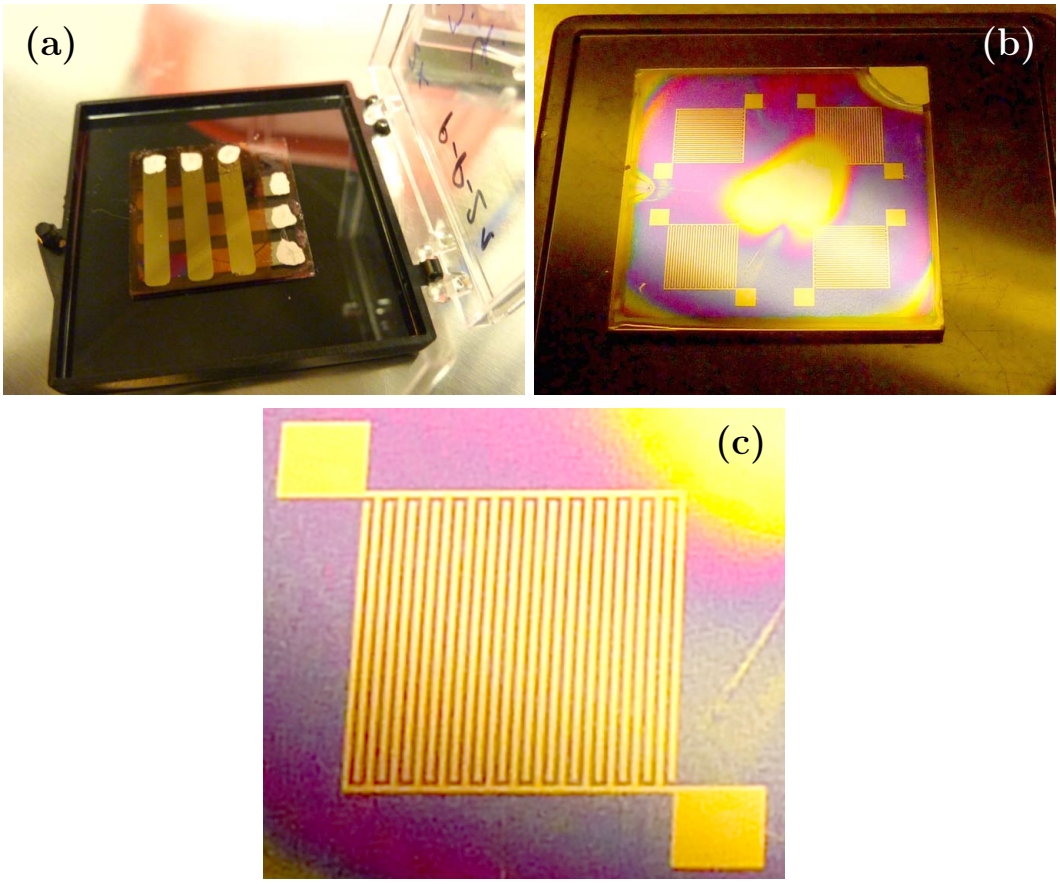

Figure 3.4: (a) Photograph of MIS device with dots of silver pain at the electrode contacts. (b) Substrate that hosts four individual FET. (c) Blow up of one FET section, showing finger structure of source and drain electrodes as well as square shaped contact areas. FET channel parameter: effective width W = 18.85 cm, length L = 100 μm

like electrode geometry was obtained by covering the ITO substrate with three stripes of Tesa-tape before they were placed into an $HCl(1mol/L) : FeCl_3$ bath at 60°C for about 5 minutes.[4] After the etching the tape was removed and the substrates were again subjected to the cleaning procedure, which was just described. The resulting bottom electrodes were smaller than the evaporated Al electrodes, leading finally in combination with the top Au electrode to an effective electrode area of around 3.2 mm × 1.7 mm.

The MIS and SMIM devices, used for the study in chapter 4, had typical insulator and semiconductor film thicknesses of around 0.25 μm...0.3 μm and 0.05 μm, respectively.

Based on the leakage currents, presented in Fig. 3.8 (page 39), an insulator film thickness of around 0.25 μm presents the optimum between low operation

[4]The etching procedure was conducted by courtesy of Patric Pingel and Frank Jaiser from the group of Prof. Neher at the University of Potsdam.

voltage of the electronic devices on one side and reliable insulating properties on the other side.

The FeFETs were prepared either onto substrates with an evaporated Al layer or onto a cleaned ITO substrates. For the ITO devices no etching was performed, i.e. the entire area was covered with ITO as bottom-gate electrode. The spincoating of the P(VDF-TrFE) and P3HT layer was performed as for the MIS devices, described above. Insulator film thicknesses between 0.1 μm and 0.5 μm were prepared. The preparation was concluded with the evaporation of the top Au source and drain electrodes of 4 individual FET transistors. All FeFETs were manufactured in a class 10000 micro-fabrication clean room at the Fraunhofer Institute. For transport and storage the devices were kept under a nitrogen atmosphere.

Each of the transistor source and drain contacts consisted of a fine lamella (or finger) structure gearing into each other and creating thereby an effective channel width of W = 18.85 cm and channel length of L = 100 μm. Fig. 3.4(b) shows a FET device (hosting four individual FETs) with a bottom Al electrode. The blow up in Fig. 3.4(c) depicts the finger structure, leading to the relatively high effective channel width.

The FeFET, used for the measurement in section 4.4, had film thicknesses of 0.3 μm and 0.05 μm for insulator and semiconductor, respectively.

3.2 Characterization Methods

The section below provides descriptions of experimental techniques and setups, which are frequently applied in the course of this thesis.

3.2.1 Determination of Film Thickness

All film thickness were measured with the 'Dektak 3 ST' surface profiler. Hereunto, reference samples of P3HT and P(VDF-TrFE) layer were prepared in parallel with the actual devices (FET, MIS etc.) and with identical spin coating parameters. After drying, the film of the reference sample was scratched (down to the glas substrate) with a sharp scalpel. The measurement of the topology perpendicular of the scratch at (at least) three different positions yielded the finally average film thickness of the film. To ensure a reliable operation, the surface profiler had to be turned on, for warm up, 10-15 min before the start of the actual measurement.

3.2.2 Impedance Measurements

Dielectric measurements were performed with the Novocontrol Alpha A impedance analyzer in conjunction with a Novocontrol broadband high voltage booster (HVB 300). The dielectric setup with impedance analyzer, HVB 300, cryostat, N_2-dewar and computer is shown in Fig. 3.5(a) and (b). In order to ensure temperature stability as well as a uniform heating of the sample, the device was placed into a cryostat under a constant flow of nitrogen. The temperature of the sample and the flow of nitrogen were controlled by a Novocontrol Quatro Cryosystem. For the measurement the sample was positioned onto a sample holder and connected through brass contacts, given Fig. 3.5(c), with HI and LO to bottom and top electrode of the MIS device, respectively. The temperature at the sample was measured with a PT100 temperature probe, situated at the sample holder. The data acquisition and the operation of the setup was realized with the Novocontrol WinDETA software.

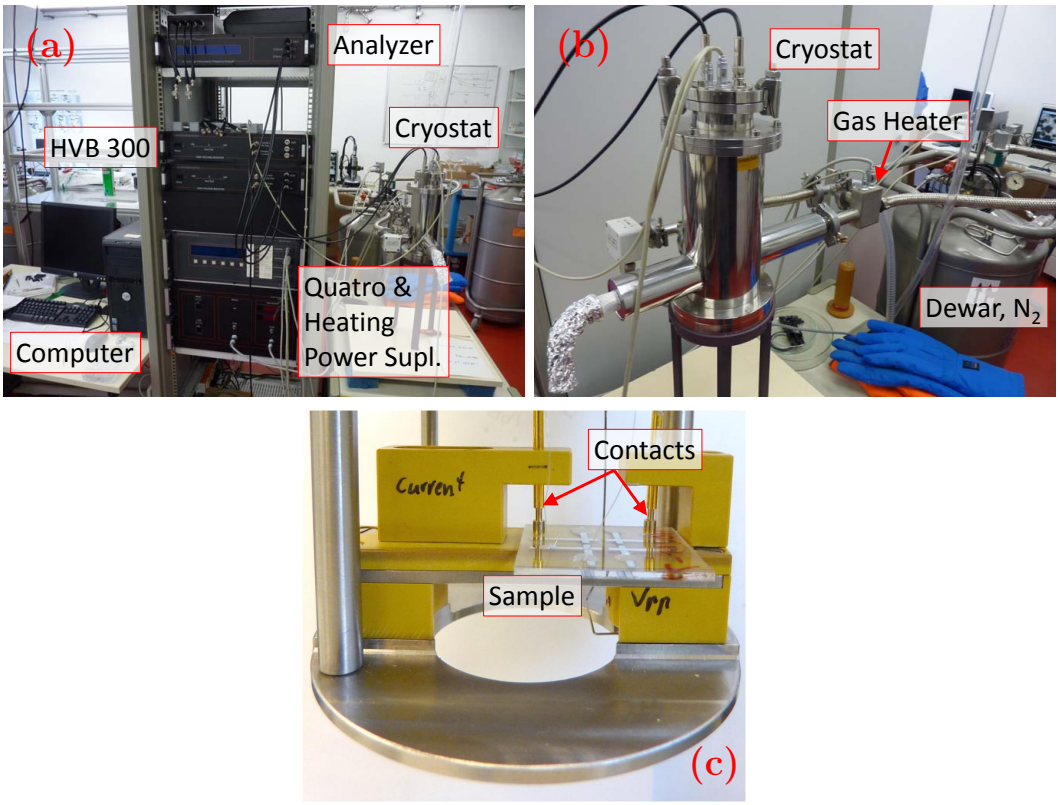

Figure 3.5: Dielectric setup (a) with close-up of the cryostat-dewar unit (b). (c) Close up of Sample and sample holder, used for the dielectric and TSC measurements.

3.2.3 Field-Effect Transistor Measurements

FET characteristics were measured with an Agilent 4155C Semiconductor Parameter Analyzer from Hewlett Packard.[5] For the measurement the device was placed onto a measuring station and electrically connected with graphite tips. All measurements were performed inside a nitrogen glove box. The setup was operated through a LabView program.

3.2.4 Thermally Stimulated Current Measurements

Thermally stimulated currents (TSC) were measured with a Novocontrol setup. In this setup the MIS device was placed into a cryostat and kept under a flow of nitrogen. The temperature of the nitrogen and sample was controlled by a Novocontrol Quatro Cryosystem. The Cryostat and Quatro was similar to that used for the impedance measurements (refer to Fig. 3.5(a)-(c)). The voltage supply and current measurement were realized with a Keithley 6517 electrometer. All components were operated through the Novocontrol WinTSC software.

3.2.5 Current-Voltage Measurements

The setup for the current-voltage measurements consisted, among other parts, of function generator (HP 33120A), for the generation of the voltage pattern and multimeter (HP 24401A) for the measurement of the generated voltage function. The generated voltage pattern was amplified by a 100V power source, which was connected in series to another multimeter (HP 3458A) and the sample. The core of the voltage amplifier was a PA98 power-operation amplifier from APEX Micro-Technology with effective 100 V output and bandwidth of 150 kHz. The polarization current, influenced by the applied voltage, was measured directly with the multimeter (HP 3458A), which was series connected to sample and power source. For data acquisition and controlling, both multimeter as well as the function generator were connected to a computer with a *TestPoint* program. The actual applied voltage was calculated from the output given by the HP 24401A by means of a calibration factor. In order to avoid interfering signals the sample holder was enclosed by a grounded Al housing, which could also be flooded with nitrogen for measurements on air sensitive samples.

[5]The FET measurements were conducted by courtesy of Prof. Neher at the University of Potsdam.

3.3 Fundamental Device Characterization

The quality of the surface, which was shown in Fig. 3.2(b) , and the electrical properties such as the ferroelectric polarization is important for the operation of devices based on MIS structures. For instance a high leakage current will make it impossible to analyse the output as well as transfer characteristics of FeFETS. Quantities such as the remanent polarization and permittivity might also be needed for the correct interpretation of the C-V curves of MIS devices and the characteristics of the FeFETs in the following sections. It is therefore worthwhile to further characterize the P(VDF-TrFE) layer.

Another important point is the identification of parasitic effects in the C-f measurements of MIS structures.[94,126] This phenomenon is caused by lateral currents along the insulator/semiconductor interface and may cause a loss peak at low probing frequency. To avoid the misinterpretation of parasitic effects, for instance, as loss peaks associated to interface traps, section 3.3.2 presents an analysis of the MIS structure in terms of this phenomenon. Section 3.3.2 has been published as listed in the references.[51]

3.3.1 Characterization of Ultra-Thin Poly(vinylidenefluoride-Trifluoroethylene) Films

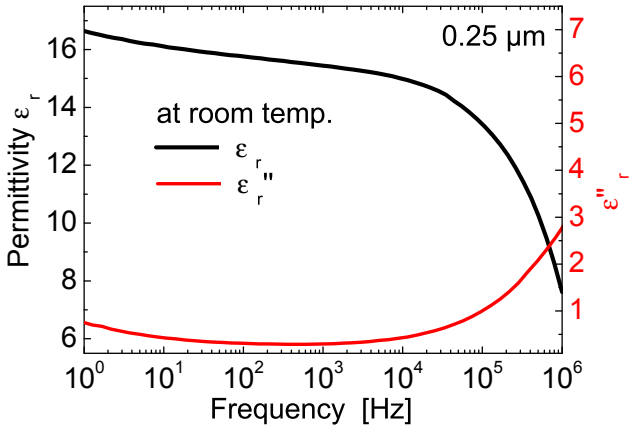

Figure 3.6: Spectra of the real and imaginary part of permittivity of an 0.25 μm thick P(VDF-TrFE) layer with top and bottom Al electrodes. Measuremet was taken at room temperature.

The complex permittivity as function of frequency for a 0.25 μm thick P(VDF-TrFE) film is given in Fig. 3.6. Here, the real and imaginary part is labeled as ε_r and ε_r'', respectively. Above 10^5 Hz the measured real part of the relative permittivity gradually increases from 14 to wards almost 16 and thus compares to values found by Furukawa *et al.*[34] The onset of the visible relaxation towards higher frequencies and the concomitant decrease in capacitance could be attributed to the α_a, i.e. glass transition of P(VDF-TrFE),[34] as well as the contact resistance which was found to be $\approx 100\ \Omega$. The latter effect can be basically understood as an interface or Maxwell-Wagner

effect, caused by the resistance of the contact electrodes R_{el} and the capacitance of the insulating layer C_i.

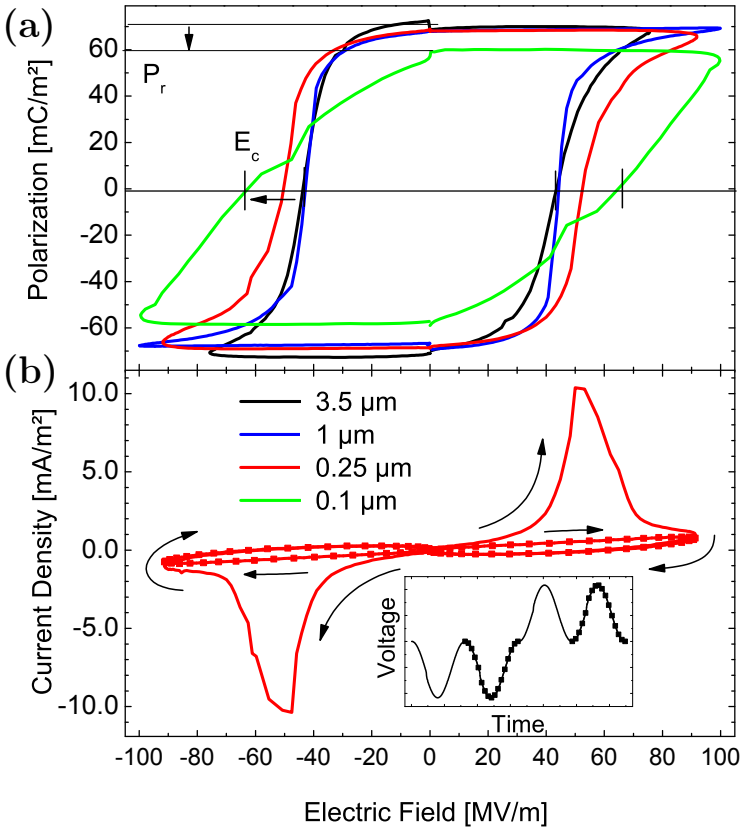

Figure 3.7: Hysteresis plots (a) retrieved from current voltage characteristics of MIM devices with P(VDF-TrFE) film thicknesses of 3.5 μm, 1 μm, 0.25 μm and 0.1 μm. (b) Polarization current density of 0.25 μm thick P(VDF-TrFE) layer as function of a sinusoidal uni/bipolar voltage pattern (given in the inset). Al was used as electrode material. The frequency of the entire cycle was 0.008 Hz. For 0.1 μm thick films, remanent polarization P_r decreases slightly. Gradual, increase of coercive field E_c for film thicknesses < 1 μm.

Fig. 3.7 (a) shows the hysterical behavior of the polarization of P(VDF-TrFE) films for different layer thicknesses, retrieved from current voltage (I-V) measurements. In Fig. 3.7 (b) an I-V characteristic is exemplarly shown as measured on MIM devices with a 0.25 μm thick P(VDF-TrFE) film by means of a uni/bipolar voltage loop. The Hysteresis curves were measured at a frequency of 0.008 Hz.[6]

Two points emerge from the data. Firstly, the remanent polarisation P_r decreases slightly to 60 mC/m^2 for the 0.1 μm thick P(VDF-TrFE) layer. Whereas, down to film thicknesses of 0.25 μm, the remanent polarization is

[6]Here, the frequency refers to the entire uni/bipolar voltage cycle, which corresponds to a measurement time of about 2 min.

around 70 mC/m^2. Secondly, an increase of the coercive field E_c from 48 MV/m, for film thicknesses of 3.5 μm and 1 μm, towards 65 MV/m for the 0.1 μm thick P(VDF-TrFE) film. Such a decrease of P_r and increase of E_c for ultra thin films has been reported by Xu *et al.*[138] and Naber *et al.*[77] Both authors relate this thickness dependency of P_r and E_c mainly to the decrease of crystallinity with film thickness.

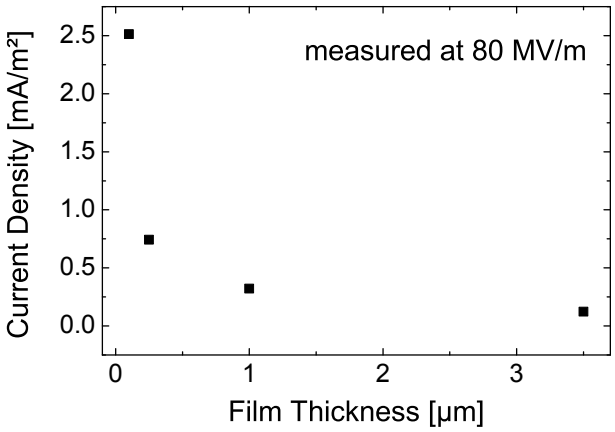

Figure 3.8: DC leakage current measured at 80 MV/m for different film thicknesses. Al was used as electrode material.

The hysteresis curves suggest that the spin coated films with thicknesses down to 0.1 μm can be remanently polarized. However, it is also noticeable that the hysteresis curve for the 0.1 μm thick film shows a more 'rhomboid' like shape. This effect indicates that the saturation regime was not reached during the poling, a problem related to the increase of leakage current in thin films, shown in Fig. 3.8. A further increase of voltage would have caused electrical breakdown, i.e. short circuit (SC), of the MIM devcie. This was eventually the reason to use insulating layers with a thickness of around 0.25 μm in most of the studied MIS and FET devices. At this point a layer thickness of 0.25 μm represents lowest possible film thickness, which can be reasonably used for the preparation of our organic electronic devices. Hence, further decrease of thickness, leads to an increase of leakage current and to an elevated probability of SCs in the MIS and FET devices. Some authors[48] suggest the application of an additional thin blocking layer to avoid such problems, a solution that requires further optimization.[40] Gelnick *et al.* has shown that it is indeed feasible to produce 0.15 μm thick insulating layers with relatively low leakage currents in the nA region. Thus, the preparation of thin films may be further improved in future studies.

3.3.2 Lateral Current Inspection in MIS Structures

Introduction

Dielectric studies of the MIS structure, as given in Fig. 3.9, yield detailed information about the state of the insulator/semiconductor interface. Capacitance-voltage (C-V) and capacitance-frequency (C-f) measurements provide, for instance, information about the density and kind of charges stored at the interface as well as the existence of interface states.[2,96,115,131] However, the interpretation especially of C-f spectra may be difficult. Relaxations due to interface states, for example, can be mistaken for interface effects such as the Maxwell-Wagner relaxation.[52,126,131]

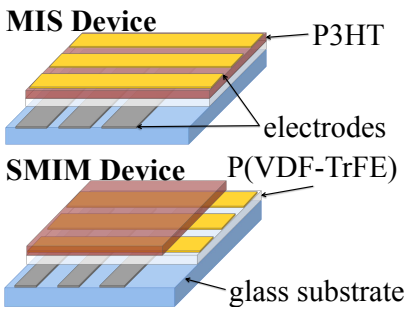

Figure 3.9: Diagrams showing the structure of the MIS (TOP) and the SMIM (BOTTOM) device.

The latter effect is caused by the series combination of the insulator capacitance with the semiconductor capacitance and resistance, which may result in relaxations in the low and mid-frequency range. On the other hand, relaxations caused by interface states are due to the interaction of charges with interface traps.[115] Relaxations at low frequencies may also arise from parasitic effects, caused by lateral currents.[47,93,94] These parasitic effects can also be considered as Maxwell-Wagner-like relaxations, but this time caused by the charging of the area around the electrode ΔA with the corresponding capacitance ΔC_i.

The identification of these effects is important in order to avoid misinterpretation of the measured C-f and C-V data. The frequency at which lateral currents may cause a relaxation in the C-f spectra largely depends on the device geometry, its preparation and processing details. An array consisting of capacitors, as in Fig. 3.9, yielded a relatively large number of capacitors per sample. This was advantageous since it enabled measurements to be made on a large number of capacitors, thus enabling the identification of anomalies related to individual defective devices. However, the lack of a guard electrode could lead to an undefined lateral current along the bottom electrode, as shown in Fig. 3.10(b) because in these structures the lateral current spreading length L was restricted by the resistance of the semiconductor and semiconductor/insulator interface and not by the geometry of a guard electrode as in other studies.[126]

To identify possible parasitic effects in the capacitance spectra of the MIS device, a semiconductor-metal-insulator-metal (SMIM) structure, as shown in Fig. 3.9, was also subjected to C-f measurements. Both MIS and SMIM devices

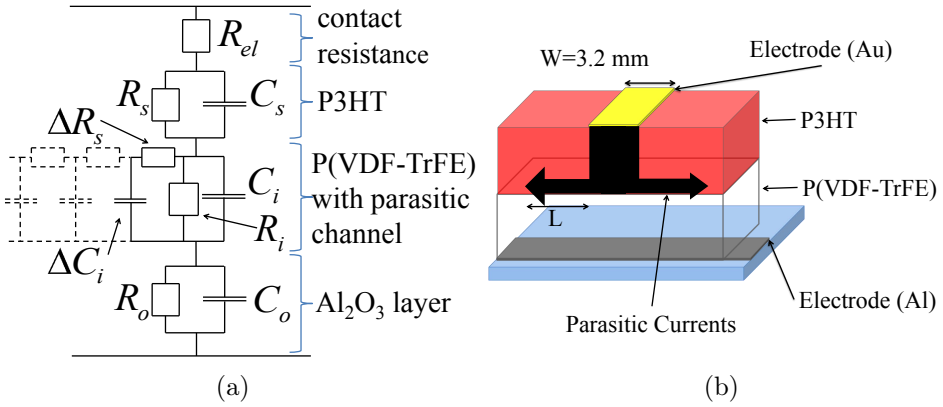

Figure 3.10: Equivalent circuit of a MIS capacitor with parasitic channel (a) together with a diagram of the device electrodes and flow of parasitic current as it spreads along the insulator/semiconductor surface (b).

have the same electrode geometry. Since the Au electrode in the SMIM device is evaporated directly on the insulator, effects caused by lateral currents will be enhanced, whereas transversal effects of the P3HT/ P(VDF-TrFE) interface will be reduced. A comparison of the C-f data of the MIS and the SMIM makes it feasible, therefore, to identify lateral parasitic effects in the spectra.

Since the insulator shows a strong ferroelectric effect, it could be assumed, that the parasitic effect also depends on the previously applied voltage. That is to say, capacitance spectra of MIS devices, taken with no applied gate voltage during the measurement, might still show strong parasitic effects in the measurements due to the maintenance of a permanent accumulation state in the device. In order to study this effect, capacitance spectra of the MIS and SMIM devices were taken at zero bias, after the application of (a) positive and (b) negative voltage.

The measured C-f characteristics of the MIS device were interpreted with the equivalent circuit, depicted in Fig. 3.10, which shows also a diagram of the electrode geometry and associated lateral currents in the sample.[47,115,126] This representation, in principle, is based on the models given in Fig. 2.7 (page 14) as well as Fig. 2.13 (page 23) and is similar to an approach utilized by Nicollian and Goetzberger.[94] The circuit in Fig. 3.10(a) models the MIS capacitor as a series combination of the semiconductor capacitance C_s and the insulator capacitance C_i. The capacitance of the aluminium oxide layer C_o, which might have formed on the back electrode, was also considered. Furthermore, the equivalent circuit in Fig. 3.10(a) modeled the ohmic resistance of insulator, semiconductor, oxide layer and the contact electrode with R_i, R_s, R_o and R_{el}, repectively.

In order to model parasitic effects caused by lateral currents, a series combination of capacitance ΔC_i and ohmic resistance ΔR_s was introduced. The

approach with a single parasitic channel constitutes an approximation, which was sufficiently good to model the position of the related relaxation process. A more correct approach, which may fit the exact shape of the relaxation, would have included a distribution of such channels.[47,126]

The capacitance beyond the electrode ΔC_i was given by

$$\Delta C_i = \varepsilon_0 \varepsilon_i \frac{\Delta A}{d_i} = \varepsilon_0 \varepsilon_i \frac{W \times L \times 2}{d_i}. \tag{3.1}$$

This capacitance was assumed to charge, due to the lateral spreading of charges along the interface, hence, was a function of the spreading length L and the electrode width W.

Further, it was assumed that charges could travel laterally through the P3HT bulk as well as through the channel, formed by the accumulation zone at the interface.[47,126] Hence, the corresponding channel- and bulk resistance R_{ch} and R_b respectively, are in parallel and yield an effective parasitic resistance $\Delta R_s = R_{ch} R_b / (R_{ch} + R_b)$. Following the approach given by Taylor *et al.*,[126] the field dependent channel resistance for a device operated in the linear regime as well as the bulk resistance is given by

$$R_{ch} = \frac{L}{W} \left(\frac{C_i}{A} V_{bias} \mu_{ch} \right)^{-1} \quad \text{and} \quad R_B = \frac{L}{W} \left(d_b N_A q \mu_b \right)^{-1}$$

respectively.

When operating in depletion mode, the film thickness of the semiconductor d_s will be reduced by the depletion zone d_d, hence the effective bulk thickness is $d_b = d_s - d_d$. However, when the device is driven in accumulation, the width of the accumulation zone is negligible, so that $d_b = d_s$.

Measurement & Discussion

Fig. 3.11 shows the C-f data obtained from the MIS device, at 0V after it had been driven into accumulation and depletion with voltages of −15V or +15V, respectively. Major differences are seen in both the loss and capacitance, especially in the low frequency region below 1 Hz.

After the device had been driven into accumulation the loss spectrum showed a prominent peak at 0.1 Hz which coincided with a strong increase in capacitance. However, measurements taken after the application of the depletion voltage showed a shift of the relaxation towards lower frequencies. It is also seen that below about 1 Hz this relaxation is superimposed on a rising background loss caused by the ohmic resistance of the insulator.

The bias of ±15 V was chosen for these measurements so as to only decrease the accumulation of the device and so shift the relaxation towards lower frequency. This made it possible to show how the 0.1 Hz relaxation

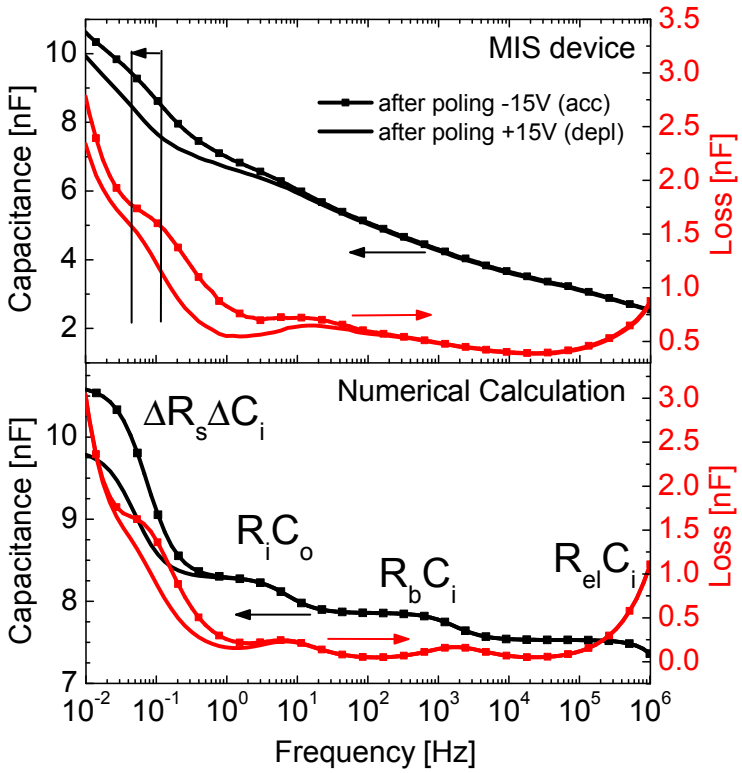

Figure 3.11: (TOP) Capacitance spectra measured at zero voltage, after biasing the MIS device into accumulation and into depletion. (BOTTOM) Calculated spectra of the MIS device based on the model in Fig. 3.10(b) and the parameters in Table 3.2. Each process in the calculated spectra is labeled with an approximate of its characteristic relaxation time, based on the equivalent circuit in Fig. 3.10(b).

depended on the previously applied voltage. A larger bias would have caused the relaxation to shift to frequencies below the measurement range.

The C-f spectrum showed two Maxwell-Wagner relaxation processes, one at 10 Hz and one at 1 kHz. The former is probably caused by the insulator resistance R_i and the capacitance C_o of the oxide layer on the Al electrode. The peak at around 1 kHz is due to the combination of the semiconductor resistance R_s and the insulator capacitance C_i.

The influence of lateral currents on the capacitance spectra of a MIS capacitor were calculated by means of the equivalent circuit, given in Fig. 3.10(a). For comparison, in Fig. 3.11 the results of the calculations are plotted together with the measured spectra. The computation of the spectra with the parameters given in Table 3.2, yielded all the main features of the measurement discussed above.

The fit is not perfect because of two main simplifications. First, the frequency dependent parameters, such as for instance the dielectric constant of P(VDF-TrFE) and the mobility of the P3HT,[98] were assumed to be constant. Since the insulator capacitance was chosen to fit the low frequency part, the

Table 3.2: Parameters used for the calculation of the capacitance spectra in Fig. 3.11.

Parameter Name, Variable	**Value**
electrode area, A	3.2×3.2 mm^2
oxide thickness, d_o	6 nm
insulator thickness, d_i	0.25 μm
semiconductor thickness, d_s	0.05 μm
oxide layer capacitance, C_o	150 nF
insulator capacitance, C_i	9 nF
semiconductor capacitance (acc.), C_s	180 nF
oxide layer conductivity, σ_o	667 pS/m
insulator conductivity, σ_i	0.6 pS/m
semiconductor bulk mobility, μ_b	1×10^{-9} m^2/Vs
semiconductor channel mobility, μ_{ch}	3×10^{-9} m^2/Vs
semiconductor doping concentration, N_a	10×10^{22} 1/m^3
bias voltage, V_{bias} (acc.)	15 V
bias voltage, V_{bias} (depl.)	5 V
spreading length, L (acc.)	0.5 mm
spreading length, L (depl.)	0.3 mm

calculated capacitance was overestimated at higher frequencies. Second, the relaxations were modeled with single characteristic relaxation time instead of a distribution. Therefore, the loss peaks appear sharper in the calculation than in the measured spectra.

Despite the approximations in the model it was still possible to interpret the measured spectra and to analyse the influence of the lateral currents on the C-f measurements. After the device was driven into accumulation, the increase of effective electrode area ΔA, caused by the lateral currents, leads to an increase in capacitance ΔC_i and to the loss peak at 0.1 Hz. When the voltage was reversed, the channel conductivity and the length L decreased, which caused the loss peak to shift to lower frequencies and the capacitance to decrease.

Due to the dependence of ΔC_i on the channel length L, as given in equation (3.1), ΔC_i was fitted by adjusting L. The spreading length L mainly changed the effective area and hence changed the capacitance and the resistance ΔR_s. The bias V_{bias} and the mobility, on the other hand, only changed the channel resistance and so ΔR_s. Hence, the mobility and the bias were used to adjust the characteristic frequency,[47] given by $\Delta R_s \times \Delta C_i$. Since the applied bias was zero during the measurement, V_{bias} was considered to be an effective voltage at the insulator/semiconductor interface, induced by the ferroelectric nature of P(VDF-TrFE), which enabled the insulator to retain its state of

polarization.

Thus, it was assumed that, when the MIS device was biased with −15 V into accumulation, that this state was retained after the bias was removed. In other words, the flat-band shift caused by polarization in the P(VDF-TrFE)/P3HT based MIS devices,[80] did not keep the device in full depletion reversing the voltage but only acted to reduce V_{bias}.

It was found that the low frequency peak is caused by lateral currents, which spread beyond the electrode area by 0.5 mm and 0.3 mm with respect to the previously applied bias of −15V and +15V. Hence, biasing the device into accumulation increased the conductivity thus causing the spreading length to increase to 0.5 mm. Biasing the device into depletion, however, lead to a effective reduction of the field at the insulator/semiconductor interface and a decrease of conductivity and hence spreading length to 0.3 mm.

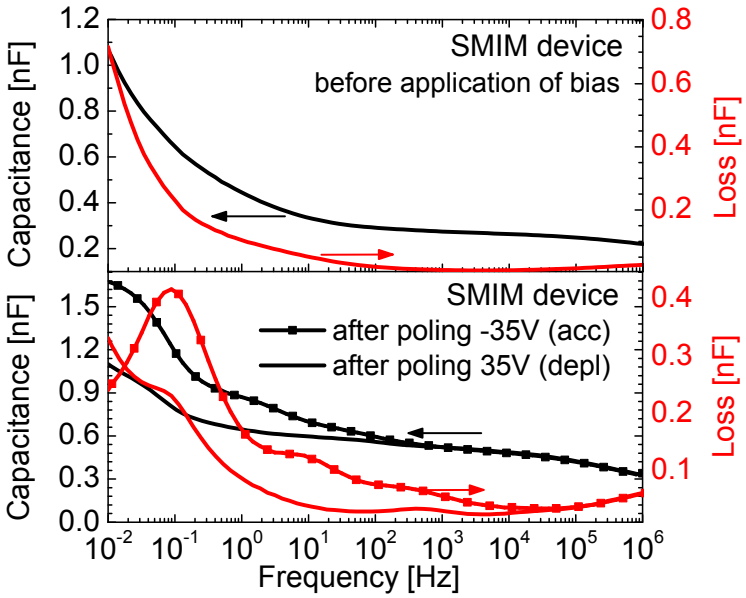

Figure 3.12: Frequency dependence of capacitance and loss for a SMIM device before (TOP) and after (BOTTOM) poling with ±35 V.

In order to verify the origin of the low frequency peak at 0.1 Hz in the C-f measurements of the MIS devices (Fig. 3.11), capacitance spectra of the SMIM devices were taken at zero gate voltage before the application of any bias (Fig. 3.12 TOP) and after biasing into depletion and then accumulation with a voltage of ±35 V. Interestingly, before the application of bias, no low-frequency relaxation was observed in the spectra. After the application of bias, however, the measurements showed a strong low frequency relaxation at 0.1 Hz and less pronounced loss peaks at around 10 Hz and 100 Hz.

Therefore, it is seen that after biasing both types of device into accumulation, the measurements revealed a peak at the same frequency of 0.1 Hz. This low frequency peak at 0.1 Hz appeared to be more pronounced in the

capacitance spectra of the SMIM device in Fig. 3.12 than in the spectra of the MIS device, shown in figure 3.11. The geometry of the SMIM device suggested stronger influences of lateral currents on the spectrum rather than of transversal interface effects. Therefore, is concluded that the most prominent peak at 0.1 Hz was entirely caused by lateral effects.

After driving the device into depletion, the low frequency relaxations at 0.1 Hz and 10 Hz shifted towards lower frequencies. Hence, the loss peak found at 0.1 Hz in accumulation shifted out of the measurement range while the 10 Hz peak was shifted to 0.1 Hz.

It was not possible to clearly identify the less pronounced loss peaks above 1 Hz. The relaxation at 10 Hz could have been caused by Maxwell-Wagner relaxations induced by the insulator and the oxidized back Al electrode. It is also possible that the P3HT around the Au electrode had some inhomogeneities, resulting in different conductivities, which would in combination with the insulator lead to Maxwell-Wagner-like relaxations at different frequencies.

Conclusion

The calculated spectra of the MIS device as well as the measurements on the SMIM lead to the conclusion that the low frequency peak at around 0.1 Hz was caused by lateral effects and led to an increase of 10% in the measured capacitance of the MIS device at low frequency. Due to the ferroelectric nature of the insulator the device area beyond the electrode was kept in accumulation or driven further into the depletion, depending on the previously applied voltage. Based on the model, it was also found that the relaxations at 10 Hz and 1 kHz were due to Maxwell-Wagner effects at the semiconductor/insulator as well as the insulator/aluminium oxide interfaces, respectively.

These findings show that the used MIS devices yield reliable capacitance spectra for frequencies above 1 Hz without effects from lateral currents, which becomes relevant in the subsequent capacitance measurements of this device. The possibility of the presence of a small MW effect at 10 Hz may not pose a general problem for the capacitance studies, however, it needs to be considered by the determination of fast interface traps in section 4.3.[113] There, the aluminium electrode is replaced by an indium tin oxide electrode, to avoid such problems arising from aluminium oxide.

4 Ferroelectric Polarization in a MIS Device

4.1 Influence of Remanent Polarization of the Insulator on Maxwell-Wagner Effect at Semiconductor/Insulator interface.

In section 3.3.2 it was shown, that the parasitic (lateral) currents only affect the capacitance spectra for probing frequencies below 1 Hz. Hence, spectra at higher frequencies may still be studied without interference from such lateral processes. The relaxation at $\approx 10^3$ Hz in the mid-frequency region of the spectra in Fig 3.11 (page 43) was interpreted as Maxwell-Wagner effect arising from the charging of the semiconductor/insulator interface. In the section below, the capacitance spectra of a MIS device with a P(VDF-TrFE) insulator, were measured under different biases, showing the effect of charge accumulation and depletion on the Maxwell-Wagner peak. The position and height of this peak clearly indicates the lack of stable depletion behavior and the decrease of mobility when increasing the depletion zone width, i.e. upon moving into the P3HT bulk.

Introduction

The mid-frequency range of capacitance spectra of MIS devices may be adequately modeled by the circuit given in Fig. 4.1.[37,113,124,131] This circuit is almost identical to the one given in Fig. 3.10(a) (page 41) but neglects influences from parasitic current and the Al_2O_3 layer. With the circuit in Fig. 4.1 it is possible to understand the appearance of the strong peak in the mid-frequency region as a Maxwell-Wagner (MW) relaxation at the semiconductor-insulator interface. The semiconductor bulk is described by a parallel branch of capacitance C_b and resistance R_b. The depletion zone and the insulator are modeled with the capacitances C_d and C_i, respectively. The resistances in these layers R_i and R_d shall not be considered in the following discussion, since they are several magnitudes higher than in the semiconductor bulk and will therefore

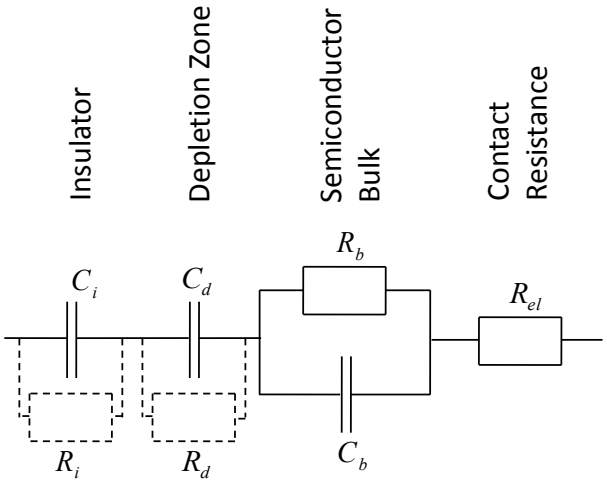

Figure 4.1: Equivalent circuit representing the contact resistance R_{el}, semiconductor bulk C_b-R_b, depletion zone C_d-R_d and insulator C_i-R_i.

only lead to an increase of loss in the low frequency region of the spectrum. They are mentioned here for completeness sake and may be used later to fit the low frequency behavior of the loss spectra. Also neglecting the contact resistance R_{el}, for the moment, the impedance Z_{MIS} and the capacitance C_{MIS} for the circuit in Fig. 4.1 can be found as

$$\begin{aligned} Z_{\mathrm{MIS}} &= \frac{1}{\mathbb{i}\omega C_{\mathrm{MIS}}} = \frac{1+\mathbb{i}\omega R_b\left(C_b+C^*\right)}{\mathbb{i}\omega C^* - \omega^2 C^* C_b R_b} \\ C_{\mathrm{MIS}} &= \frac{\omega^2 R_b^2 C^* C_b\left(C_b+C^*\right) + C^* - \mathbb{i}\omega C^{*2} R_b}{1+\omega^2 R_b^2\left(C_b+C^*\right)^2} \\ &\text{with} \quad C^* = \frac{C_d C_i}{C_d+C_i} \quad \text{and} \quad \sqrt{-1} = \mathbb{i}. \end{aligned} \tag{4.1}$$

A prominent feature in the spectra of organic based MIS devices is the MW relaxation, caused by the combination of two different layers, the insulator and the semiconductor, and is usually found between 10^3 Hz and 10^5 Hz. The position of this relaxation peak is determined by the characteristic time of the system to charge the interface through the semiconductor layer. Utilizing Equ. (4.1) it is found that this relaxation occurs at the characteristic frequency of

$$\omega_{mw} = \frac{1}{\tau_{mw}} = \frac{1}{R_b\left(C^*+C_b\right)}. \tag{4.2}$$

The bulk resistance R_b and the depletion zone capacitance C_d strongly depend on the applied bias to the MIS device. As the MIS device is driven from accumulation into depletion, the width d_d of the depletion zone increases. Hence, depletion zone capacitance, bulk capacitance and bulk resistance can be expressed through[131]

$$C_d = \varepsilon_s\varepsilon_0\frac{A}{d_d}, \; C_b = \varepsilon_s\varepsilon_0\frac{A}{d_s-d_d} \text{ and } R_b = \rho_s\frac{d_s-d_d}{A} \tag{4.3}$$

with A as the device area, ε_0 as the permittivity of free space as well as d_s, ρ_s and ε_s as the thickness, resistivity and relative permittivity of the bulk semiconductor, respectively. With these dependencies of C_d, C_b and R_b on the depletion zone width d_d, it is possible to discuss the effect of accumulation and depletion on the capacitance spectra of the MIS device, modeled with Equ. (4.1).

The depletion zone width can be varied between $d_d \longrightarrow 0$ for accumulation and $d_d \longrightarrow d_s$ for full depletion of the MIS device. Utilizing Equ. (4.3) it can be seen that, the position of the MW peak, given with Equ. (4.2), depends on the applied voltage, i.e. the characteristic relaxation frequency can be varied between the limits[131]

$$\begin{array}{ccccccc} \text{Accumulation} & & & & & & \text{Depletion} \\ \omega_{mw}(d_d \to 0) & < & \omega_{mw}(d_d) & < & \omega_{mw}(d_d \to d_s) \\ \dfrac{1}{R_b\left(C_i + C_b\right)} & < & \dfrac{1}{R_b\left(C^* + C_b\right)} & < & \dfrac{1}{R_b C_b} \\ \dfrac{1}{\rho_s \frac{d_s}{A}\left(C_i + \varepsilon_s\varepsilon_0 \frac{A}{d_s}\right)} & < & \dfrac{1}{R_b C^* + \rho_s\varepsilon_s\varepsilon_0} & < & \dfrac{1}{\rho_s\varepsilon_s\varepsilon_0}. \end{array} \tag{4.4}$$

Assuming, for simplicity, ρ_s to be independent of d_d,[1] it can be seen, that the relaxation frequency increases towards a constant value $(\rho_s\varepsilon_s\varepsilon_0)^{-1}$ as the device is driven from accumulation into depletion. This is an effect arising from the impedance of the bulk capacitance C_b, parallel to the bulk resistance R_b. With Equ. (4.2) it could be argued that the relaxation time can be understood as sum of relaxation times, namely $\tau_{mw} = \tau^a_{mw} + \tau^b_{mw} = R_bC^* + R_bC_b$. When the device is driven into depletion, the majority charge carriers are 'pushed' away from the interface, i.e. the depletion zone widens and starts to act as a dielectric, described by C_d. This leads on the other side to a decrease of the effective bulk thickness $d_s - d_d$ and consequently to a decrease of bulk resistance R_b as suggested by Equ. (4.3). Hence, in deep depletion $d_d \longrightarrow d_s$ ($\Rightarrow R_b \longrightarrow 0$) leading to $\tau^a_{mw} = R_bC^* = 0$ and with that a shift of the MW peak towards higher frequencies. Physically speaking, the charging of the capacitance C^* can be performed faster due to the decreasing resistance of the semiconductor bulk R_b. However, the constant $R_bC_b = \tau^b_{mw} = \rho_s\varepsilon_s\varepsilon_0$ defines, so to say, the highest possible response time of the semiconductor-insulator system.

On top of this, an increasing depletion zone also leads to an increase of C_b towards infinity and with that $C_b^2 >> C_b$. In this limit, C_b can be neglected and C_{MIS} in Equ. (4.1) simplifies to

$$C_{\text{MIS}} \longrightarrow \frac{C^*\left(\omega^2R_b^2C_b^2 + 1\right) - \mathbb{i}\omega C^{*2}R_b}{1 + \omega^2R_b^2C_b^2}. \tag{4.5}$$

[1] This assumption might not be valid for organic semiconductors.[53,110,131,144]

With that, the capacitance of the MIS device under depletion becomes frequency independent, $\mathrm{Re}\,[C_{\mathrm{MIS}}] \longrightarrow C^*$, and the height of the MW peak in loss spectrum decreases towards zero, $\mathrm{Im}\,[C_{\mathrm{MIS}}] \longrightarrow 0$. Thus the depletion of the MIS device leads to a shift of the MW peak in the spectrum and a concomitant reduction of the capacitance in the capacitance spectrum.

In accumulation the depletion zone capacitance C_d, given in Equ. (4.3) becomes infinit[113,131], $C_d \longrightarrow \infty$ and with that $C^* \longrightarrow C_i$. With the imaginary part of C_{MIS} in Equ. (4.1) it can be seen that in this limit, at the characteristic relaxation frequency τ_{mw}, the loss peak height is given with $C_i^2/2(C_b + C_i)$. The low frequency capacitance of C_{MIS}, well below the MW relaxation, can be approximated with C_i.

Summarizing the aboves discussion, it can be noted that in theory, as the device is driven from accumulation towards depletion, the MW relaxation shifts from lower to higher frequencies with a simultaneous decrease in the loss-peak height. Hence, when the device is in full accumulation the spectrum shows an strong increase in capacitance at ω_{mw}, which is decreasing towards a nearly constant value of C^* as the device is driven into depletion.

It is further known that the conduction processes in the P3HT, but also in other organic semiconductor, is governed by charge hopping between band states.[53,70,110,144,145] Due to the energetic and spacial distribution of these states it can be assumed that ρ_s may have spatial variations leading to a dispersive charge transport in the semiconductor bulk. The characteristic charging time of the interface is than be more accurately described by a distribution of relaxation times around τ_{mw} rather than a single one. This dispersion may lead to a broadening and a decrease of the MW peak. The latter effect can be explained with the dielectric relaxation strength, which has to be preserved for this relaxation process.

Cole and Cole[19] have demonstrated, such a dispersive behavior[131] can be well described by introducing a frequency dependent, complex resistance

$$R_b \;\rightarrow\; R_b(\mathbb{i}\omega\tau_{mw})^{-\alpha}. \tag{4.6}$$

With $0 < \alpha < 1$ the broadening of the loss peak, centered at the frequency $1/\tau_{mw}$ (equ. (4.2)), may be then adjusted to fit the measured data. Although α in this case can be understood as parameter for disorder within the semiconductor, the theory[19] provides no relation of alpha to physical quantities.

So far, we have neglected R_{el}, which needs to be introduced to model resistance of the electrodes, the measurement probe of the impedance analyzer as well as the resistance of the ohmic contact between the top electrode and the semiconductor bulk material. Since R_{el} is rather small, usually around 100 Ω[58,67], the associated frequency for this relaxation is several magnitudes larger than ω_{mw} and can therefore be considered as a separate process and thus approximated as $(R_{el}C_{\mathrm{MIS}})^{-1}$ where $C_{\mathrm{MIS}}^{-1} = C_i^{-1} + C_d^{-1} + C_b^{-1}$. In the measured

spectra, the maximum of this relaxation loss peak is often out of the measurement range and, therefore, manifests just as an increase of loss towards high frequencies and a concomitant decrease in capacitance.[58,131,134]

Measurement & Discussion

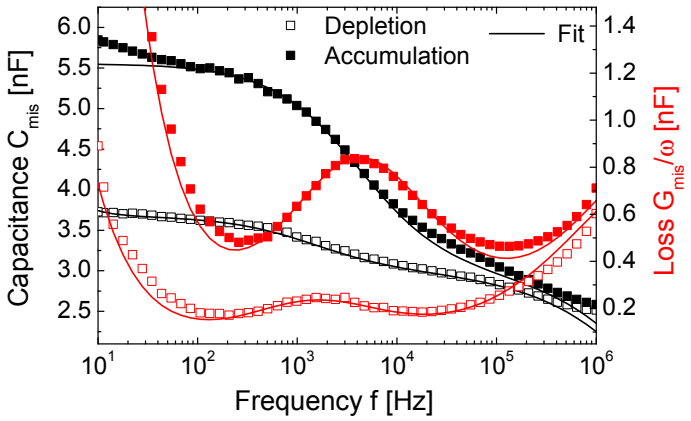

Figure 4.2: Measured (■: accumulation, □: depletion) and fit (straight line) of capacitance (black) and loss (red) spectra of MIS device. Spectra were taken under accumulation and depletion voltage of ±40 V. Fit parameters are given in Table 4.2.

Fig. 4.2 shows the capacitance spectra at accumulation and depletion voltages of −40 V and 40V, respectively. For these measurement the probing AC signal was superimposed with the DC bias. The measurement was taken under nitrogen atmosphere at a constant temperature of 20°C. The measured device was prepared with a bottom aluminium electrode, a ≈ 0.25 μm thick P(VDF-TrFE) as well as a 0.05 μm thick P3HT layer and a top gold electrode. Fig. 4.2 also contains the fit of the measured data with the parameters given in Table 4.1 based on the model introduced in section 4.1.

When poled with accumulation voltage of −40 V the characteristic relaxation frequency of the MW relaxation is about 3 kHz. With the used parameter $d_d/d_s = 0$ it can be concluded, that the device is in full accumulation. The estimate of the loss peak height with 1×10^{-9} F = $C_i^2/2(C_i + C_b)$ also supports this conclusion. The increase of loss towards low and high frequencies is due to the conductance of the insulating layer, modeled with an ohmic resistance R_i parallel to C_i, and the contact resistance R_{el}, respectively.

When driven into depletion with 40 V the loss peak height and the low frequency capacitance decreases and the relaxation frequency shifts to lower frequency of about 1 kHz. This decrease can be modeled with the increasing depletion zone width d_d, as discussed in the introduction, section 4.1. Although not fully, the device can be considered as well depleted, since the depletion zone accounts for 60% for the semiconductor bulk thickness. The decrease of relaxation frequency suggest a decreasing bulk mobility, rather than a constant one as discussed above. This result was also found by Torres *et al.*[131] and can be attributed to the decrease of order within the P3HT film on moving away from the interface.[53,110] The values between 3.7×10^{-6} cm^2/Vs and 1.4×10^{-5} cm^2/Vs

Parameter Name, Variable	**Value**
electrode area, A	3.2×3.2 mm^2
insulator thickness, d_i	0.25 μm
semiconductor thickness, d_s	0.05 μm
thickness ratio, d_d/d_s (acc., depl.)	0 (acc.), 0.6 (depl.)
Cole-Cole param. (Equ. 4.6), α	0.3(acc. & depl.)
insulator permittivity,[34] ε_i	13
semiconductor permittivity,[12] ε_s	3
insulator resistance, R_i	9×10^7 Ω
contact resistance,[131] R_{el}	70 Ω
semiconductor bulk mobil.,[53,110,144] (acc.) μ_b	1.4×10^{-5} cm^2/Vs
semiconductor bulk mobility (depl.), μ_b	3.7×10^{-6} cm^2/Vs
semiconductor doping concentration,[131] N_a	10×10^{23} 1/m^3

Table 4.1: Parameters used for the best fit of the capacitance spectra in Fig. 4.2. The decrease of μ_b under depletion, reflects the increase of disorder within the semiconductor, upon moving away from the interface.

compare to mobilities found for P3HT fractions with lower molecular weight, which are known to show a twisted and discorded chain conformation.[144] Hence, the decrease of charge carrier mobility within the bulk semiconductor is a result of the less efficient charge transport, i.e. a less efficient charge transfer between the conjugated chains in disordered regions of P3HT.[56,97]

Above, it was shown that the capacitance spectra and its voltage dependence can be well understood and described with the equivalent circuit in Fig. 4.1. Here, the voltage dependence was (indirectly) modeled by the introduction of the depletion zone width dependent Equ. (4.3). In theory, the depletion and accumulation state of MIS device should be preserved by the field of the remanent polarization of the insulator. It should be, therefore, also possible to see the effect of the remanent polarization on the spectra of the MIS device. A remanent depletion should in principle lead to a permanent shift of the MW peak towards lower frequencies and a concomitant decease of capacitance after the depletion voltage was removed. In order to study the effect of remanent depletion more closely the capacitance and loss spectra were measured under a sequence of biases as shown in Fig. 4.3(a) and (b), respectively. Before the measurement, the device was pooled several times with an alternating DC voltage pattern of ±25 V, which is necessary to obtain a stable ferroelectric switching behavior of the P(VDF-TrFE) insulator. At very low frequencies the voltage should drop mainly over the insulating layer. In this frequency regime both layers can be considered as a series combination of resistances, were the insulator has a much higher resistance than the semicon-

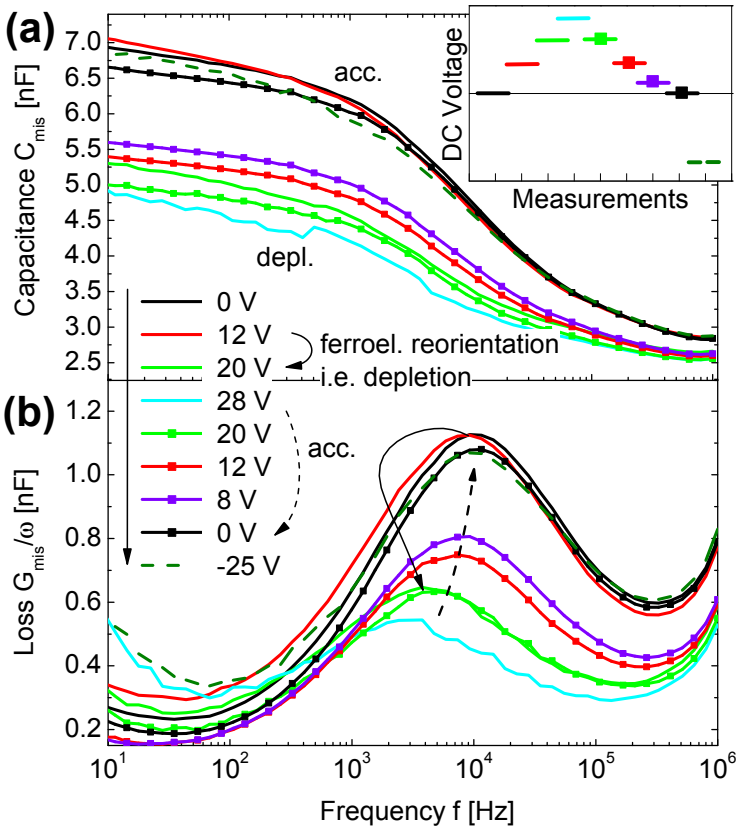

Figure 4.3: Measured capacitance (a) and loss (b) spectra of MIS device at different biases. For each frequency sweep, the voltage was increased stepwise from 0 V towards depletion voltage of 28 V and subsequently again decreased 0 V. Spectrum taken under accumulation voltage of −25V is also shown.

ductor. Therefore this DC voltage is high enough to exceed the coercive field E_c of around 60 MV/m within the P(VDF-TrFE) layer. The last poling voltage in this pattern was an accumulation voltage of −25 V. After the device was brought into this defined initial condition the actual measurement was taken.

The frequency sweeps were subsequently measured with voltages from 0V towards a depletion voltage of 28V. After that, the voltage was again stepwise decreased towards 0V. Spectra were also taken with different negative accumulation voltages. Under accumulation voltages, however, the spectrum remained almost unchanged, therefore Fig. 4.3 contains only one measurement with −25V. Since the ferroelectric insulator was poled before the measurement with a negative voltage, the device was kept in accumulation until the opposite field was reached. For the measured device, this is around ±15 V. Therefore, as the depletion voltage was increased the device remained in its accumulation state until 12 V and showed depletion behavior for 20 V and 28 V.

When the voltage was decreased again towards zero volts, it could be seen, that at 12 V the device is about to accumulate again but has not been returned

to full accumulation, at this point. It is only at the subsequent measurement at 8 V and 0 V that the MIS device is in its initial accumulation state. This sequence of measurement shows the ferroelectric insulator has an influence of the accumulation/depletion behavior. It shows that only when the coercive field in the insulating layer is reached the MIS device starts to deplete, which is reflected in a decrease and shift of the MW peak. Furthermore, the capacitance spectra show that the device is not in a stable state of depletion after depletion voltages have been applied but returns to accumulation.

The reason for this instable depletion mode can not be clearly inferred from this set of measurements. Although, the applied bias of ±20V is high enough to exceed the coercive field of 60 MV/m in the ≈ 0.25 μm thick insulator it could be concluded that the ferroelectric polarization is not stable in depletion mode.[79,80] It was argued by Naber *et al.* that the uni-polar p-type semiconductor P3HT is not able to support negative compensation charges to the interface leading to a depolarization of the ferroelectric molecular dipoles in the insulator. At first glance, this argument seems reasonable because it is supported by the finding that PVDF and its copolymers require compensation charges to maintain a remanent ferroelectric polarization.[27,28]

It is not possible to directly retrieve information about the orientation of dipolemoment and the orientational stability of a ferroelectric insulator from capacitance spectra. Therefore at this point the argumentation by Naber *et al.* could theoretically serve as a possible explanation for the measured instability. However, it shall be shown in the course of the next section that the conclusion about the depolarization is probably incorrect and that a careful study of the ferroelectric switching by means of capacitance-voltage (C-V) characteristics suggests a stable remanent polarization.

Conclusion

It was demonstrated that the capacitance spectra can be described with the model introduced in section 4.1. With this model a decrease of bulk mobility was calculated upon moving away from the interface, which is probably caused by the increase of disorder within the P3HT bulk.[53,56,97,110] By tracing the position and height of the MW peak, it was shown that the device started to deplete for voltages above $E_c \times d_i$, however, it did not remain in a stable depletion state. The origin of this instability can not clearly determined from this set of measurements and will be the subject of the subsequent sections. From the position of the loss peak, it also follows that the charges of the semiconductor bulk can only follow frequencies below 1 kHz. Hence, the full effect of depletion and accumulation on the C-V characteristic, i.e. the decrease and increase of the capacitance C_{MIS}, can only be monitored below this frequency. Furthermore, the determination of interface traps requires less corrections for

frequencies below the MW effect.[2,113] In the following sections the analysis of the C-V data was therefore always performed for low probing frequencies below 1 kHz.

4.2 Stability of Polarization in Organic Ferroelectric Metal-Insulator-Semiconductor Structures

The capacitance measurements, presented in the last section 4.1, clearly show the MIS device does not remain in a stable state of depletion. This phenomenon shall be further investigated by means of capacitance-voltage and current-voltage measurements, in the section below. It turns out that the two polarization states are stable, i.e. no depolarization occurs below the coercive field. Further, the results strongly suggest the presence of structurally fixed electrons at the semiconductor/insulator interface, compensating the effect of ferroelectric polarization of the insulator under depletion. The section below has been published as listed in the references.[50]

Introduction

MIS devices incorporating the ferroelectric copolymer poly(vinylideneflouride-trifluoroethylene) (P(VDF-TrFE)) as the gate insulator have attracted much attention for possible use in electronic memories.[16,48,62,77,80,81] Several studies[71,79] have reported on programmable, non-volatile ferroelectric-field-effect-transistors (FeFETs) incorporating
P(VDF-TrFE) as the gate dielectric. Indeed, P(VDF-TrFE) based FeFETs and MIS devices have been studied in combination with organic[71,77,124] as well as inorganic semiconductors[48,62]. The combination of P(VDF-TrFE) with the organic semiconductor poly(3-hexylthiophene) (P3HT) constitutes a good multilayer system to study ferroelectric polarization in MIS devices.[75,80,81] P3HT is a p-type semiconductor with hole mobility reported to be up to, and even exceeding 0.1 cm^2/Vs.[15,111] The capacitance of a P3HT-based MIS capacitor decreases when the applied voltage drives the semiconductor from accumulation to depletion (refer to section 2.2.1).[96,109] In the absence of interface or insulator trapped charges, this occurs at around 0 V gate bias and constitutes the flat-band voltage, V_{FB}, condition in the device. However, as already discussed in section 2.2.2, interface or insulator trapped charges give rise to a shift, V_{FB}, in the flat-band voltage.[113]

When the gate insulator is a ferroelectric, the remanent polarization should also change V_{FB} to negative (positive) voltages when the ferroelectric

is poled with accumulation (depletion) voltages.[2] Hence, capacitance-voltage (C-V) measurements offer the opportunity to measure and distinguish between different charge types at the insulator/semiconductor interface.[88,113] When the device is driven from accumulation to depletion, the remanent polarization initially maintains the device in accumulation until the coercive field E_c is exceeded at which point the ferroelectric polarization reverses and V_{FB} changes. A shift of 10 V has been reported[75,80] for a 220 nm thick P(VDF-TrFE) insulator. Important for the operation of FeFETs is that the accumulation and depletion modes of the P3HT semiconductor remain stable following the application, respectively, of negative and positive coercive electric fields to the MIS structure. However, several reports have highlighted the apparent instability of the ferroelectric polarization in P(VDF-TrFE) after poling with depletion voltages.[75,79,80] The present study re-visits this problem and concludes that previous interpretations for the loss of remanent polarization may not be correct.

It is reasonable to assume that different kinds of interface charges exist which may differ in physical properties such as polarity and electric field dependence. A distinction is made between the charge per unit area Q'_p, caused by the ferroelectric polarization, $P(E)$, and the interface trapped charge density, Q'_{T}, which is independent of the applied field E.[113] The charge $Q'_p = P(E)$ will only change for fields above the coercive field $E_c = V_c/d_i$, were V_c is the voltage appearing across the insulator of thickness d_i. Hence, the V_{FB} may be defined as

$$V_{\mathrm{FB}} = -\frac{1}{C'_i}\left(Q'_{\mathrm{T}} + Q'_p\right) \tag{4.7}$$

where C'_i is the insulator capacitance per unit area.

Dickens *et al.*[21] and Bauer[7] have described a unipolar/bipolar voltage sweep method, that allows the contribution of re-orienting dipoles in the ferroelectric to be removed from its current-voltage (I-V) characteristic.[66] Since the mathematical expression for the current can be rewritten as an expression for capacitance, such a technique should also be applicable to capacitance measurements. Hence, neglecting ohmic contributions, the measured current density $J_m = \mathrm{d}Q'/\mathrm{d}t$ and the measured capacitance per unit area $C'_m = \mathrm{d}Q'/\mathrm{d}V$ are

$$J_m = C'_i\frac{\mathrm{d}V}{\mathrm{d}t} + \frac{\mathrm{d}P}{\mathrm{d}t} \quad \text{and} \quad C'_m = C'_i + \frac{\mathrm{d}P}{\mathrm{d}V} \tag{4.8}$$

where P is the ferroelectric polarization (in *charge per unit area*). C'_i represents the purely capacitive contribution ($C' = \varepsilon_0\varepsilon_r/d_i$) where ε_r is the dielectric constant related to C'_i, ε_0 the permittivity of free space and $\mathrm{d}P/\mathrm{d}V$ the contribution from the changing ferroelectric polarization. Therefore, a reversal of the

[2] Please, refer to page 17 in section 2.2.1 for more detail.

ferroelectric polarization when the coercive field is exceeded during an initial voltage sweep will manifest itself as a peak in the C-V plot as well producing a shift in V_{FB}.[16,80] The onset of depletion may be determined, therefore, either by the effective interface charge ($Q'_p + Q'_{\mathrm{T}}$) through equation (4.7) or by the change in ferroelectric polarization at $V_c = E_c d_i$. The distinction between V_c and V_{FB} is necessary, since V_c is determined only by the coercive field E_c which is independent of both the polarization $P(E)$ and the charge Q'_{T}. Hence, V_c cannot be used to calculate the density of interface charges. When a second unipolar sweep is undertaken,P remains unchanged and no peak in capacitance will be observed, even though the coercive field is exceeded. The onset of depletion is now determined by $(Q'_p + Q'_{\mathrm{T}})$.

Consequently, if two unipolar voltage loops are applied to a ferroelectric, only the first will contribute to switching of the ferroelectric dipoles.[21] Thus, the state of polarization of the gate insulator of a MIS capacitor may be determined either from the appearance of maxima in the C-V plot or from shifts in V_{FB}. Furthermore, as will be shown in the following, this approach allows ferroelectric polarization to be distinguished from other charge trapping effects.

Measurement & Discussion

The studied devices had typical insulator and semiconductor layer thicknesses of around 0.3 μm and 0.06 μm. The results of the present investigation are exemplified by Fig. 4.4. The I-V and C-V characteristics of our MIS capacitors using the approach of Dickens *et al.*[21] are shown in Fig. 4.4(a) and (b), respectively. It is evident that both the capacitance and current measurements yield corresponding dependences on the applied voltage. The change of polarization of the insulator $\mathrm{d}P/\mathrm{d}V$, given in Equ. (4.8), leads to a peak in both the current and the capacitance when the coercive field is reached[16] - but only during the first-half cycle as the voltage increases towards $\pm V_{max}$. On the back sweep to zero voltage and in subsequent unipolar sweeps, all dipoles in the insulator bulk maintain their new orientation so that no peaks related to ferroelectric switching occur in either the I-V or C-V plots.

The I-V plots are now composed simply of displacement ($C'_i \mathrm{d}V/\mathrm{d}t$) and leakage currents, while the C-V plots exhibit a continuous decrease from accumulation to depletion. Therefore, it can be concluded concluded that the ferroelectric polarization is stable until reversed by a voltage sweep of opposite polarity. This is confirmed in Fig. 4.4(c) where we show the polarization hysteresis loop constructed by integrating the current response to a complete bipolar voltage cycle in Fig. 4.4(a). Contrary to the assertion of Naber *et al.*[80], therefore, the ferroelectric remains remanently polarized even after depleting the semiconductor.

The C-V curves, however, do not exhibit the same degree of hysteresis.

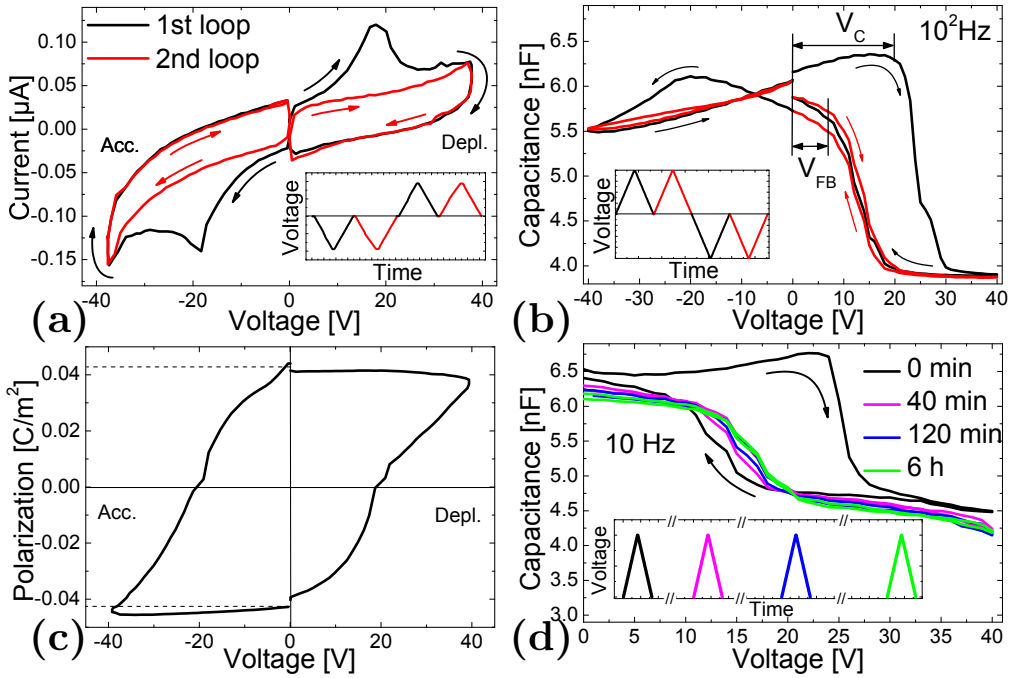

Figure 4.4: (a) I-V plots (sweep rate:1.5 V/s) and (b) C-V plots (sweep rate: 1 V/s) of a MIS capacitor with a 0.3 μm thick P(VDF-TrFE) ferroelectric insulator. The insets in (a) and (b) show the sequence of the applied unipolar/bipolar voltage sweeps in the range $V_{\max}$ = ±40 V. Reversal of the ferroelectric polarization is observed only during the first voltage sweep beyond the accumulation/depletion coercive fields. The polarization hysteresis loop derived from the I-V plot is shown in (c). As seen in (d) after polarization reversal, C-V plots are stable for at least 6 hours. The inset here shows the sequence of the applied unipolar voltage sweeps made after switching the polarization.

For the first cycle under positive bias, both the 'forward' and 'back' sweeps show a shift in the flat-band voltage, with the onset of depletion occurring at V_c = 20 V and V_{FB} = 10 V, respectively. The former is clearly associated with polarization switching of the molecular dipoles when the coercive field is reached. In the ideal case, the device should remain in depletion during the back sweep, until the applied voltage exceeds the negative coercive field which is expected to occur at about −20 V. This is clearly not the case here since $V_{\mathrm{FB}} \approx 10$ V on the back sweep and also in subsequent unipolar sweeps. Several reasons have been suggested for this positive V_{FB}.

(a) Ionic charges in the insulator may migrate to neutralise the ferroelectric polarization.[28] However, the stability of the polarization and therefore the lack of hysteresis in the unipolar sweeps taken up to 6 hours after switching the ferroelectric polarization (Fig. 4.4(d)) does not support such an argument.[66] Furthermore, a positive V_{FB} requires that the ferroelectric polarization is overcompensated by negative charges migrating through the insulator to the

insulator/semiconductor interface. Since the internal ferroelectric polarization field provides the driving force for such a process, overcompensation is unlikely to occur. Although, the presented measurements yield no further evidence for such a process, at this point, charge migration throug the insulator can not entirely excluded.[8,24]

(b) It was proposed by Naber *et al.*[75,80] that since no inversion layer forms in the p-type P3HT there is a lack of minority electrons to compensate the ferroelectric polarization leading to a partial depolarization of the P(VDF-TrFE). However, our measurements confirm that the ferroelectric polarization is stable.

(c) In an earlier publication Naber *et al.*[79] suggest that band bending in the semiconductor gives rise to a depolarizing electric field on the grounds that electron injection into P(VDF/TrFE) 'is less probable because it is a wide bandgap insulator'. As long ago as 1973, however, Pfister *et al.*[100] demonstrated that charge injection occurred from the electrodes into PVDF films with later work demonstrating that hole injection was stronger than electron injection[112] although both occur.

In our case, despite the lack of inversion charges, we believe that when P3HT is in depletion, electrons are available for injection into the insulator as reported for inorganic devices.[64,84] The recent work of Nakajima *et al.*[84] also presents evidence for the existence of charges at the interface between the p-type organic semiconductor α, ω-Dihexylsexithiophene (DH-6T) and P(VDF-TrFE). In support of our argument we note further that upon reversing the polarization with a sufficiently high depletion voltage, the P3HT layer becomes fully depleted. This occurs when the capacitance in Fig. 4.4(a) reaches a minimum[125] and is equivalent to 'punch through' in silicon devices. The field at the gold contact is then increased sufficiently to inject electrons which can drift through the semiconductor as demonstrated in recent reports of ambipolar conduction in P3HT[18] and during photoexcitation of P3HT MIS capacitors.[125] Sufficient of these electrons become trapped on insulator states to overcompensate the effect of the positive Q_p yielding a positive V_{FB}. Such a process has already been identified as a cause of depletion induced threshold voltage instability in P3HT/polyimide MIS capacitors.[132]

To determine Q'_{T} we return to Fig. 4.4(c) where the remanent polarization is estimated to be 0.04 C/m^2 and in reasonable agreement with values appearing in a previous report[80]. From the accumulation capacitance, 6 nF in Fig. 4.4(b) C'_i is estimated to be 5.86×10^{-4} F/m^2. Assuming V_{FB} = 10 V, and Q'_p = 0.04 C/m^2 in Equ. (4.7), then Q'_{T} = −0.0459 C/m^2. Although this negative charge represents a small excess over Q'_p, nevertheless, it reflects a much higher effective interface state density (2.87×10^{13} states/cm^2) than observed in non-ferroelectric insulators.[2] We conjecture, therefore, that electrons are trapped on the positively charged surfaces of ferroelectrically polarized P(VDF-TrFE)

crystallites close to the interface with the semiconductor.

Conclusion

In conclusion, it was demonstrated that, contrary to previous suggestions, the ferroelectric polarization in P(VDF-TrFE)/P3HT MIS devices is stable both in accumulation and depletion. The apparent reduction of ferroelectric polarization in depletion is due, rather, to electron transfer from the P3HT depletion region into insulator-related trap states at or near the insulator/semiconductor interface. The high density of trapped electrons is sufficient to overcompensate the ferroelectric polarization $P(E)$ leading to the suggestion that the electrons are trapped at the surface of the poled crystallites located near the interface with the semiconductor. In principle, therefore, inclusion of an electron blocking layer at the P(VDF-TrFE)/P3HT interface should prevent this effect and lead to an improved memory device.

4.3 Interface Traps at Semiconductor/Insulator interfaces

In the previous section 4.2, strong evidence about the presence of fixed negative charges was presented. However, as discussed in section 2.2.2, semiconductor/insulator interfaces may, besides fixed charges, also contain fast interface traps. The following sections shows that by means of a unipolar/bipolar voltage pattern the ferroelectric influence from the C-V data of the MIS device can be removed and that the conductance method[96,113] can be applied to determine the interface trap density. It shall be shown, the P3HT/P(VDF-TrFE) interface contains both the structurally fixed positive charges and a distribution of fast traps sites for majority charge carriers, i.e. holes.

Introduction

Interface charges have significant influence on the charge-carrier mobility in organic field effect transistors (OFETS)[143]. It is therefore important to identify those charges. The total charge density in a MIS capacitor is the sum of the space charge density of the semiconductor bulk, the interface-state charge density and the fixed charge density.[96] Interface traps (also referred to as inerface states, fast states or surface states) are energetically situated within the bandgap between the conduction and the valence band.[113] Historically this theory was used for inorganic semiconductor devices. However, Alves *et al.*[2], Torres *et al.*[131] as well as Taylor[126] *et al.* have demonstrated the application of this

theory for organic semiconductor devices. P3HT based MIS devices have been found to have interface state densities in the range of $10^{10}-10^{11}$ $(\mathrm{eVcm}^2)^{-1}$.[2,126]

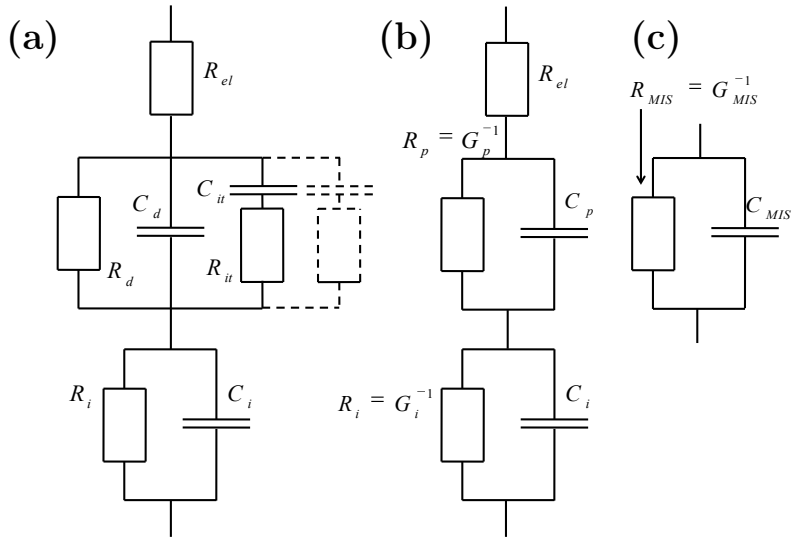

Figure 4.5: Equivalent circuit (a) modeling a MIS device (below the MW relaxation frequency) with C_i, R_i, C_d, R_d and R_{el} as insulator capacitance, insulator resistance, depletion zone capacitance, depletion zone resistance as well as a contact resistance, which in this frequency regime may also represents the bulk resistance of the semiconductor. Interface trap response is represented by a series combination of R_{it} and C_{it} yielding its characteristic response time $\tau = R_{it} \times C_{it}$. The branch modeling the semiconductor with IT can be expressed in terms of a frequency dependent capacitance and resistance, C_p and R_p, respectively (b). Circuit (c) represents the measured frequency dependent capacitance and resistance C_{mis} and R_{mis}, respectively.

The capacitance of the MIS system with interface traps C_{MIS} may be modeled by a combination of equivalent circuit as given in Fig. 4.5(a).[2,116] Each layer is represented by parallel combination of capacities and resistances, modeling the high and low frequency response, respectively. Capacitance and resistance of insulator and semiconductor depletion zone are represented as C_i and R_i as well as C_d and R_d. The interface traps (IT) are modeled as distribution of series combinations of resistances R_{it} and capacitances C_{it} leading to a continuum of interface traps, parallel with the depletion zone capacitance C_d.[96] For simplicity reasons the circuit in Fig. 4.5(a)and (b) does not explicitly contain an R-C branch representing the semiconductor bulk. When measuring at frequencies below the MW relaxation the bulk can be approximated by a resistance. Hence, in this case R_{el} presents the resistance of the semiconductor bulk as well as the resistance of the contact electrode.

When the device becomes depleted the number of charges in the semiconductor Q_s decreases leading to a decrease of $C_d = \mathrm{d}Q_s/\mathrm{d}V_s$ and with that a overall decrease of C_{MIS}. When biased into depletion C_d, which is parallel to

C_{it}, becomes small enough to detect the change of charge in the interface traps as the fermi level moves up and down with respect to the interface trap level. The presents of interface states may be identified in the loss-voltage plots as peak and in the corresponding capacitance-voltage characteristics as stretch out at the onset of depletion.

The branch presenting the semiconductor in Fig. 4.5(a) can be converted in to a frequency dependent capacitance C_p and conductance G_p as given figure Fig. 4.5(b). Neglecting the influences of ohmic conductances, the loss for a continuum of traps is given by[2,96]

$$\frac{G_p}{\omega} = \frac{AN_{ss}q}{2\omega\tau}\ln\left(1+\omega^2\tau^2\right). \tag{4.9}$$

The interface state density and their characteristic response time are given by N_{ss} and τ, respectively. It can bee seen that equation 4.9 goes through a maximum, leading to peak in the loss spectrum if $\omega\tau \approx 2$. Since τ depends exponentially on the semiconductor surface potential, i.e. band bending V_s, not only the loss-spectrum but also the loss-voltage measurement reveals a peak if $\omega\tau(V_s) \approx 2$.[96] Hence, the interface state density can be inferred from the loss maximum, which shall be denoted as $\left|\frac{G_p}{\omega}\right|_{max}$. With the electrode area A equation (4.9) yields

$$N_{ss} \approx \frac{2\left|\frac{G_p}{\omega}\right|_{max}}{q^2 A} \qquad \left[\left(\mathrm{eVcm}^2\right)^{-1}\right]. \tag{4.10}$$

As discussed in section 2.2.3, the surface potential $V_s(V_g)$ as function of applied gate voltage V_g can be calculated from the low-frequency capacitance $C_{lf} = \mathrm{d}Q_s/\mathrm{d}V_g$ with[96]

$$V_s(V_g) = \int_{V_{\mathrm{FB}}}^{V_g}\left(1-\frac{C_{lf}}{C_i}\right)\mathrm{d}V_g + V_s(V_{\mathrm{FB}}). \tag{4.11}$$

Before G_p/ω could be extracted, it was also necessary to correct the measured capacitance for the contribution of the ohmic conductance. It was therefore assumed to have ohmic conductance $R_{mis}(V_g,\omega)$ parallel to the capacitance C_{mis} as shown in Fig. 4.5(c).[127] In this case the measured loss is given by $1/\omega R_{mis}(V_g,\omega)\omega$. [3]

The resistance $R_{mis}(V_g,\omega)$ can be inferred from the DC current, measured during the C-V measurement. A first-order correction can then be performed

[3] In the low frequency limit, the DC contribution of the loss is related to the insulators and semiconductors resistance with

$$\frac{1}{R_{mis}(V_{\mathrm{acc}},\omega)\times\omega} = \frac{1}{\omega\times R_i} \quad \text{in accumulation and}$$
$$\frac{1}{R_{mis}(V_{\mathrm{depl}},\omega)\times\omega} = \frac{1}{\omega\times(R_i+R_d)} \quad \text{in depletion.}$$

by calculating the $R_{mis}(V_g, \omega)$ for accumulation and depletion voltage and subtracting the corresponding constant ohmic loss contribution from the measured data in accumulation and deletion mode, respectively.[2] These two voltages have to be chosen appropriately on either side of the loss peak. The transition from accumulation to depletion is then approximated with a linear decreasing contribution. Subsequently, G_p/ω can be retrieved by correcting with the data for the reactance of C_i with the Conductance Method, a procedure described in detail by Nicollian and Goetzberger.[96]

The studies on MIS devices with Al electrodes, in section 3.3.2 showed the presence of a loss peak at around 10 Hz, which was probably caused by a MW effect at the AlO_2/P(VDF-TrFE) interface. In order to avoid influences from this kind of interface effect, it was decided to use ITO instead of Al as bottom electrode. Negative influences from such a phenomenon on the below presented measurements can be therefore excluded.

Measurement & Discussion

As discussed above (and section 2.2.2), the presence of interface states can be identified by a characteristic peak in the loss spectrum when the device switches from accumulation towards depletion mode. The identification of these states can, however, be difficult if the gate insulator is ferroelectric. Figure 4.6 shows capacitance and loss characteristics of a P(VDF-TrFE) sample with a layer thickness of ≈ 0.3 μm. The applied unipolar/bipolar voltage is shown in the inset. It can be seen that the capacitance as well as the loss curves peak at the first half of the first cycle when the coercive field is reached and the molecular domains are reoriented. On the second sweep however all ferroelectric domains are oriented and therefore no peak is observed.

Figure 4.7 shows capacitance and loss characteristics of a MIS device also measured with a unipolar/bipolar voltage cycle.[4] The loss curves in Fig. 4.7(b) reveal a strong non ohmic conductivity contribution. Especially in accumulation the conductivity shows an increase towards higher voltages. In depletion this influence is less pronounced, due to the formation of the depletion layer.

On the first cycle the capacitance as well as the loss curves reveal a peak, caused by the ferroelectric switching. In the loss curve under accumulation voltage this effect is less eminent due to the high conductivity. However, in depletion, the ferroelectric peak makes it difficult to clearly identify and determine the position and magnitude of the actual interface loss peak. When the coercive field in the insulator is reached, the reorientation of the ferroelectric domains and the depletion of the MIS device occur simultaneously.

[4] The devices was prepared with an ITO bottom electrode. The Insulator and semiconductor layer had a thicknesses of around 0.3 μm and 0.06 μm. For preparation details refer to section 3.1.3.

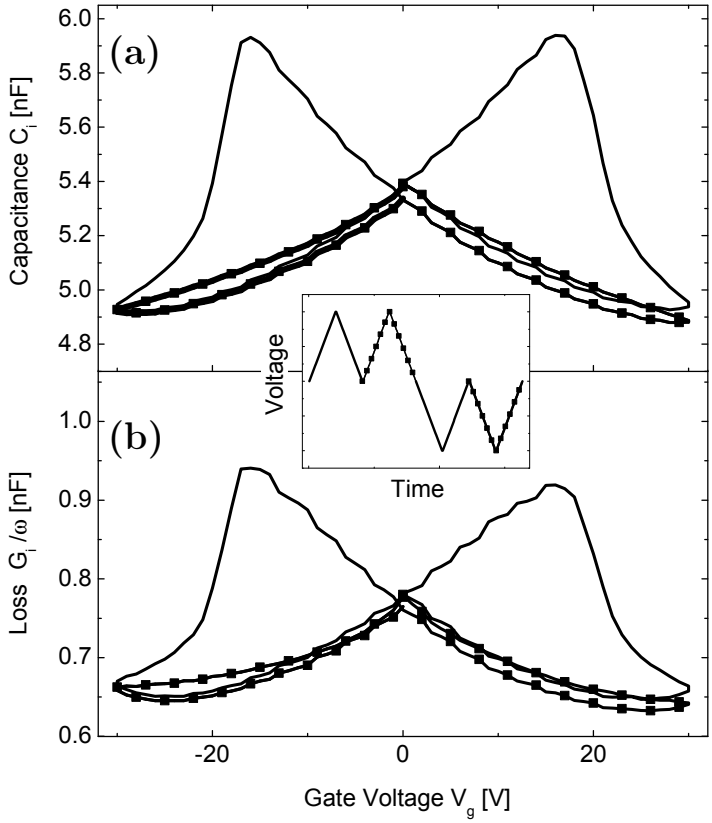

Figure 4.6: Capacitance C_i (a) and Loss G_i/ω (b) vs. gate voltage of 0.3 μm tick P(VDF-TrFE) layer measured at 1 kHz. Peak at $\approx$ 15 V clearly indicates reorientation of the ferroelectric domains on the first voltage cycle (straight line), described dP/dV (see Equ. 4.8). The second cycle (■ symbols) is dominated by the linear response of the insulator. Applied unipolar/bipolar voltage cycle is given in the inset.

For the analysis it was therefore decided to use the loss curve measured during the second cycle. Since all the ferroelectric domains became remanently oriented during the first cycle, the peak at around 5 V can not be due to the ferroelectric switching. The loss curves were measured at frequencies above 1 Hz and below 1 kHz. Hence, influences of lateral currents which was shown to take place for frequencies below 1 Hz, can be neglected.[51,126] Maxwell-Wagner relaxation of P3HT based MIS devices takes place at frequencies above 1 kHz[132], therefore influences due to the slow response of the semiconductor layer can also be excluded from further discussions. Hence, the loss peak should be due to interface traps only.

Fig. 4.8(a) shows the measured loss curves for depletion voltages. Especially the curves below 80 Hz show a strong conduction contribution to the loss, which increases with increasing voltage. The results of the conductivity correction, as described in above, is given in figure 4.8(b). Here it can bee seen that after the correction the background, which was increasing with towards

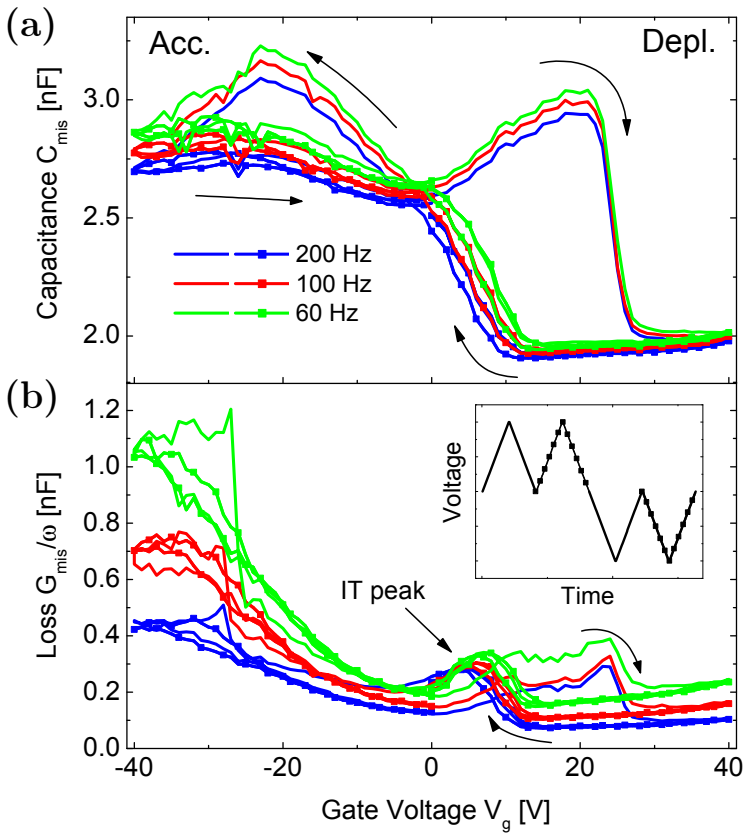

Figure 4.7: Capacitance C_{mis} (a) and loss G_mis/ω (b) vs. gate voltage of the MIS device, measured at 200Hz (Blue), 100Hz (Red), 60Hz (Green). Inset shows unipolar/bipolar voltage pattern. Second cycle is marked with ■ symbols. Back sweep of the first positive voltage cycle as well as subsequent second cycle reveals peak due to interface (IT) traps at ≈ 5 V.

lower frequencies, has been removed. Since the peak position is around 5 V, the corrections were made for accumulation and depletion values at 0 V and 15 V, respectively.

Only the low frequency curves Fig. 4.8(b) reveal an increase of conductivity with increasing depletion voltage i.e a non ohmic behavior. The subsequent correction for the reactance of the insulator with the Conductivity Method is given in Fig. 4.8(C). With Equ. (4.9) the peak heights can now be related to the interface-trap density N_{ss}. The second cycle of the low frequency capacitance curve measured at 20 Hz can further be used to calculate the integral in equation 4.11. The onset of depletion, i.e. the the flatband condition occurs at V_g = 5 V, which was used to determine the integration constant $V_s(V_{\mathrm{FB}})$. The evaluation of the inequation $\omega^2 C_i^2 > R_i^{-2}$ (derived in section 2.2.2 on page 22), with the values ω = 20 Hz, C_i = 2.5^{-9} F and R_i = $9 * 10^7$ Ω (latter value taken from Table 4.1 on page 52) shows that the insulator resistance allows the use of Equ. 4.11. The plot of the interface trap density N_{ss} vs. the semicon-

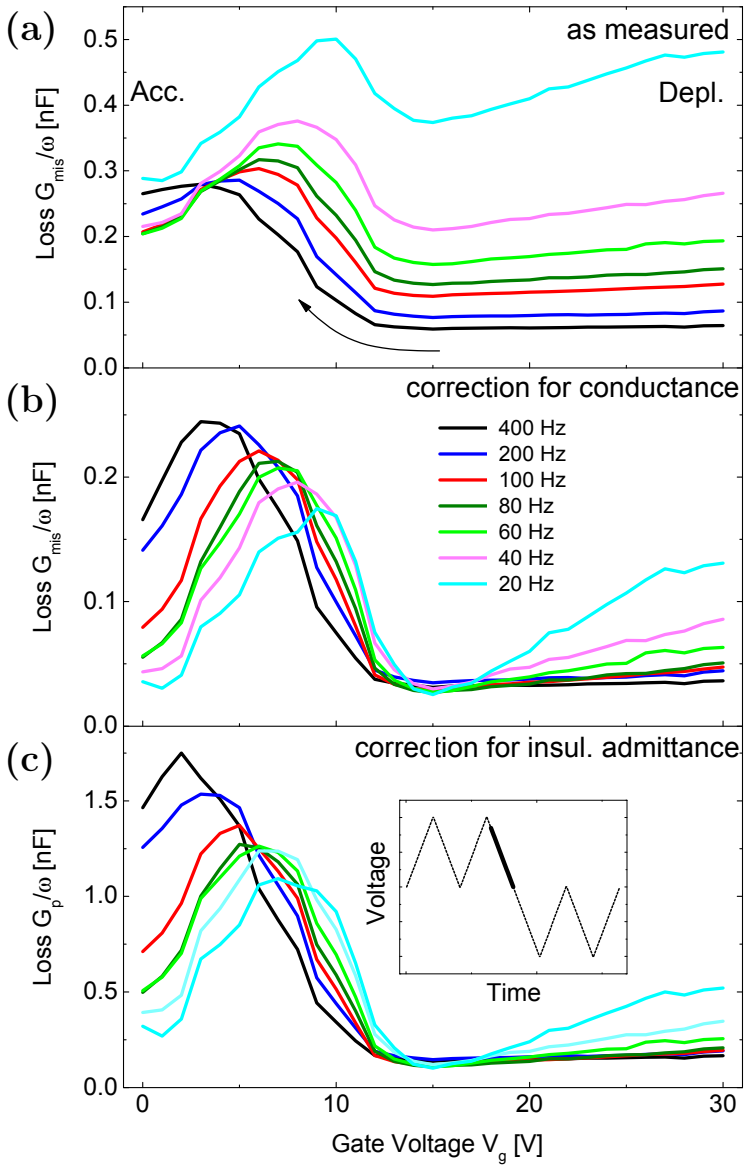

Figure 4.8: Loss characteristics of MIS device as measured (a), after DC correction (b) and after correction with Conductance Method[96,113] (c), measured at 400 Hz, 200 Hz, 100 Hz, 80 Hz, 60 Hz, 40 Hz and 20 Hz. Curves were measured a the back sweep of the second positive cycle as indicated in the inset.

ductor surface potential V_s can be found in Fig. 4.9. The inset shows $V_s(V_g)$ as it was calculated with Equ. (4.11). The red curve indicates the part of the second cycle, used for plot of $N_{ss}(V_s)$. The values of N_{ss} are in the range of 10^{11} $(\mathrm{eVcm}^2)^{-1}$ and increases towards lower semiconductor surface potential. Thus, the calculated interface state densities are in the same order of magnitude as found in other publication for P3HT MIS systems ($10^{10} - 10^{11}$ $(\mathrm{eVcm}^2)^{-1}$).[2]

The origin of these hole trapping states can not entirely inferred from the measurements and an explanation can therefore only be speculative.[96,113]

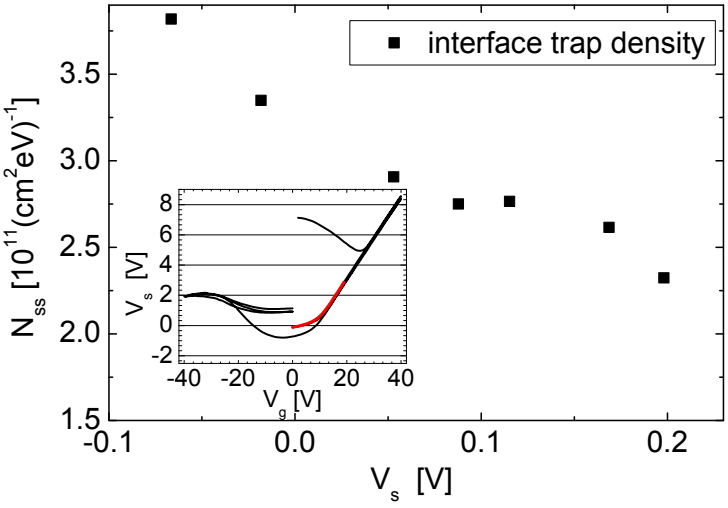

Figure 4.9: Interface trap density N_{ss} as function of the surface potential $V_s(V_g)$. Inset shows the $V_s(V_g)$ calculated with equation 4.11 for the entire unipolar/bipolar voltage sweep (Black) and the part which was used in the plot N_{ss} vs. $V_s(V_g)$ (Red).

However, in the last section 4.2 it was shown that there is strong evidence for the existence of structurally fixed negative charges at P3HT/P(VDT-TrFE) interfaces.[50,84] These negative charges overcompensate the ferroelectric polarization. Hence, they are not compensated by other positive charges near the insulator interface and may therefore act as trap sites for majority charge carriers. Another possible explanation for those shallow traps could be on the other side structural imperfections at the interface.

Conclusion

In conclusion, it was shown that after the removal of the ferroelectric influences of the insulator from the measured loss and capacitance characteristics, the conductance method[96,113] can be applied to determine the interface trap density. The P3HT/P(VDF-TrFE) interface contains a distribution of interface trap sites of around 10^{11} $(\mathrm{eVcm}^2)^{-1}$, which is in the same order of magnitude as found for other organic P3HT based MIS systems.[2,126] Hence, the P3HT/P(VDF-TrFE) interface contains, beside the structurally fixed positive charges (see section 4.2), also a distribution of fast traps sites for majority charge carriers, i.e. holes.

4.4 Effect of Stable Ferroelectric Polarization on the Field-Effect Transistor Performance

The section below presents a study of the effect of a remanently polarized insulator on the performance of field effect transistors. In its course evidence will be presented supporting the idea that electrons become permanently trapped during the first poling cycles. This process leads to a permanently altered conductance of the insulator/semiconductor interface. The measured output

characteristics also confirm the assumption, developed at the end of section 4.2, that electrons become trapped on the positively charged surfaces of ferroelectrically polarized P(VDF-TrFE) crystallites at the insulator/semiconductor interface.

Introduction

Ferroelectric field effect transistors based on the ferroelectric P(VDF-TrFE) (FeFET), have been studied in recent years by Reece *et al.*[103], Naber *et al.*[79–81] and others.[16,62,133] They have shown that P(VDF-TrFE) is a good candidate for non-volatile memory applications. In the previous section, strong evidence was presented that the ferroelectric insulator remains in a stable polarized state during the depletion. It is therefore not the depolarization of the insulator, as suggested by Naber *et al.*[80], but trapped negative charges at the semiconductor/insulator interface that leads to a lack of remanent depletion of the MIS device.

A trapping of negative charge during the poling of the MIS device, implies that the insulator/semiconductor interface changes its conductivity during the first poling cycles. Since, the trapped negative charges can be considered as structurally fixed, this change of conductivity should be permanent and not be reversible by any accumulation voltage. Such a process, however, is difficult to monitor in a C-V measurement. In order to become a clear C-V reading, the device has to be subjected to a couple bipolar voltage sweeps, at the first measurement, to obtain a collective orientation of the ferroelectric domains. The capacitance of the P(VDF-TrFE) layer, i.e. the capacitance of the MIS device, changes rapidly during this 'run-in' procedure leading to noise in the C-V reading. Therefore measurements on FeFETs were preformed as shown in Fig. 4.10. Fluctuations of the insulator capacitance have minor effects on the DC current characteristics of this type of measurement.

Experimental & Discussion

In order to study the accumulation and depletion behavior of the FeFET during the first poling cycles, $I_{\mathrm{D}}(V_{\mathrm{DS}})$ was measured with a uni/bipolar drain voltage pattern as depicted in Fig. 4.10. The application of two subsequent unipolar loops, denoted as (C1) and (C2), allows to identify possible influences from the ferroelectric switching on the $I_{\mathrm{D}}(V_{\mathrm{DS}})$ as well as on the gate current I_{G}.

Each bipolar half cycle (labeled as (P1),(P2),...) leads to a depletion for negative drain voltage and accumulation for positive drain voltages. Since V_{GS} = 0 V the application of a drain voltage will also induce a field between drain and gate contact. The case of accumulation and depletion with the respective current directions is also given in Fig. 4.10. In depletion, positive

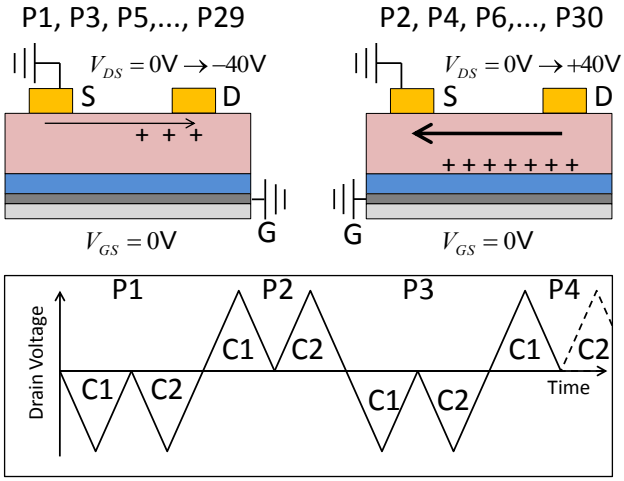

Figure 4.10: Poling procedure used for the measurement of the output characteristics. Negative/positive voltages correspond to depeletion/accumulation of the device. Each bipolar cycle is labeled as (P1), (P2) et cetera. Odd ((P1),(P3),...) and even numbers ((P2),(P4),...) correspond to negative and positive drain voltages respectively.

charge carriers are pulled away from semiconductor/insulator interface leading to a negative current reading at the drain contact (D). This current flow is then from source (S) towards the drain (D) contacts and mainly governed by conduction processes through the semiconductor bulk. When driven into accumulation, holes become injected through the drain contact[5] causing, consequently, a positive drain current reading. Hence, positive or negative drain current readings refer to currents of positive charge carriers, from or towards the drain contact, respectively.

Due to the nonlinear behavior of the insulator during the reorientation of the ferroelectric domains it is not possible to describe the output characteristic analytically. A complete description would require a numerical solution as suggested by Miller *et al.*[71]. However, based on the studies of the MIS-device, it is still possible to discuss the results qualitatively and to obtain an understanding about the physical processes, even without a numerical fit. Furthermore, the application of uni/bipolar voltage sweeps allows the separation of the pure capacitance part as discussed in the previous section.[7,21] Hence, with this separation, an analysis by means of Equ. (2.29) and (2.30) remains possible.

In Fig. 4.11(a) and 4.12(a) a selection of output characteristics is given for negative and positive drain voltages, respectively. Here, the drain currents were measured as function of the bi/unipolar drain voltage cycles shown in Fig. 4.10. Both Fig. show plots of the first (C1) and the second (C2) unipolar cycle, for each poling direction ((P1), (P2),...). In the course of this measurement the poling direction was altered thirty times starting with negative poling voltages

[5]The drain acts in this case as the source for holes. It should also be mentioned that, since absolute potential values can be shifted for convenience, the poling schemes can be translated. The one on the left hand side in Fig. 4.10 with V_{GS} = 0 V and V_{DS} = 0 V → −40 V is equivalent to V_{GS} = 40 V and V_{DS} = 40 V → 0 V. The one on the right hand side with V_{GS} = 0 V and V_{DS} = 0 V → +40 V is equivalent to V_{GS} = −40 V and V_{DS} = −40 V → 0 V.

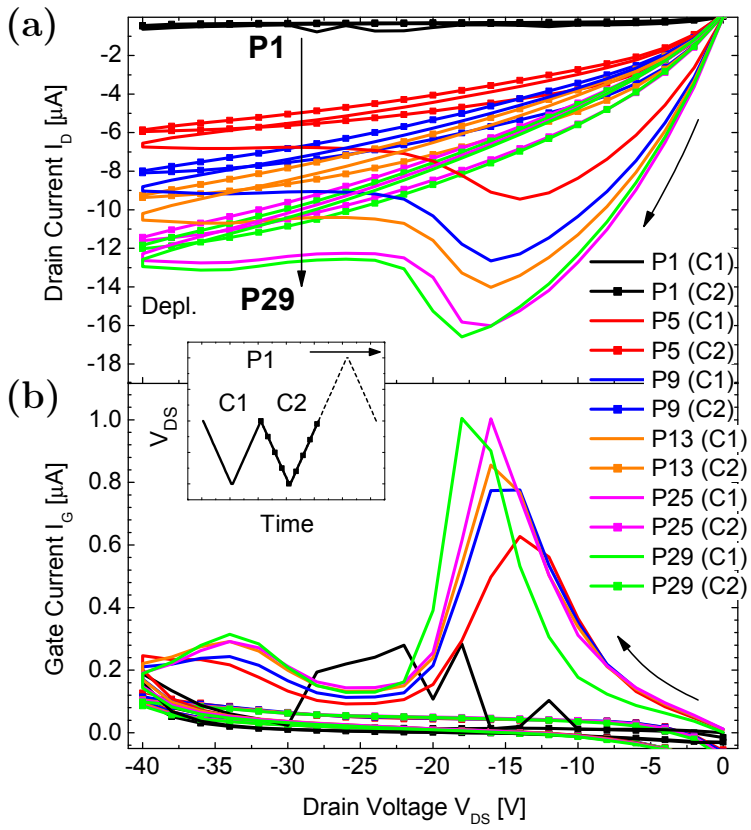

Figure 4.11: Selection of (a) output characteristics for negative (depletion) drain voltages (as depicted in the inset) and (b) associated gate currents measured as function of drain voltage pattern given in Fig. 4.10. Both uni-polar cycles, (C1) and (C2), are shown for the corresponding negative poling cycles (P1), (P5), (P9), (P13), (P25), (P30). Complementary measurement for positive drain voltages is given in Fig. 4.12.

(P1), followed by a positive poling (P2) and so on.

Fig. 4.11(a) shows an increase of drain current for each poling step. During the first poling into depletion (P1) the max. current is $I_D(V_{DS} = -40\ \text{V}) \approx 5 \times 10^{-7}$ A, however, increases rapidly during the subsequent poling steps. At the poling (P5) the drain current starts to saturate and for the poling cycles (P25) and (P29) the drain currents of $I_D(V_{DS} = -40\ \text{V}) \approx 12 \times 10^{-5}$ A, are almost identical. The corresponding gate currents, given in Fig. 4.11(b), show a clear current peak associated to the ferroelectric switching as well as an almost constant leakage current in the order of 10^{-8} A..10^{-7} A. Hence, the increase of drain current upon the poling cycles (P1) to (P29) can not be explained by an increase of leakage current through the insulator, but rather, has to be caused by an increase of conductivity of the interface. It also shows that this process of increasing conductivity starts to saturate after the device became poled 5 times into each direction, which corresponds to the growth and final

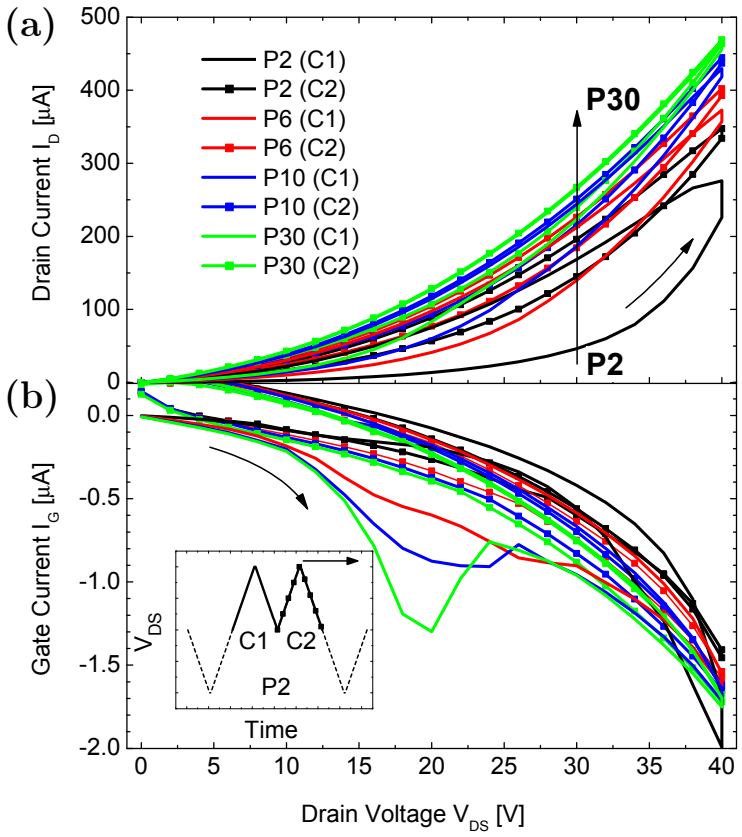

Figure 4.12: Selection of (a) output characteristics for positive (accumulation) drain voltages (as depicted in the inset) and (b) associated gate currents measured as function of drain voltage pattern given in Fig. 4.10. Both uni-polar cycles, (C1) and (C2), are shown for the corresponding negative poling cycles (P2), (P6), (P10), (P30). Complementary measurement for negative drain voltages is given in Fig. 4.11.

saturation of polarisation peak height in the gate current. This growth in peak height indicates a build up of ferroelectric polarisation in the P(VDF-TrFE) layer over many cycles.

Although, such a behavior has been noticed for P(VDF-TrFE) capacitors, at this point it is not entirely clear how this increase of ferroelectric polarisation could be explained in detail. However, a similar phenomenon was reported by Guy *et al.*[39] for PVDF and attributed to the conformational transition of the crystal structure of Form II (α- PVDF) towards Form I (β- PVDF). The studies of Reynolds *et al.*[104] on P(VDF-TrFE) on the other side might lead to the conclusion that this built up of polarization is attributed to the alignment of ferroelectric domains by the electric field. Based on this, it could be theorized that during the first cycles the movability of the ferroelectric domains has been increased, leading to a gradual increase of polarization.

This set of measurement in Fig. 4.11(a) finally shows that the interface of the FeFET has been altered permanently. Indeed the second cycle (C2) shows

always a lower saturation drain current compared to the first one (C1). However, this decrease is relatively small compared to the increase of conductivity from (P1) to (P29) and probably indicates a further depletion of the interface. It is obviously not possible to completely reverse this increase of conductivity.

Although, this can not serve as a prove, it may still yield strong evidence for the trapping of negative charges during the first poling cycles promoting the accumulation of holes and a concomitant increase of conductivity of the interface in depletion mode. It was theorized in the last section that these negative charges might be stabilized or trapped by the positively charged surfaces of ferroelectrically polarized P(VDF-TrFE) crystallites close to the interface. The correspondence of saturation of interface conductivity to the saturation of polarisation peak height in the gate current is evidence for the correctness of this theory. Hence, the results support the idea, developed in the last section, about negative charges, which become trapped and (so to say) fixed at the interface during the measurement.

Furthermore, the effect of the ferroelectric switching is visible in the drain as well as in the gate current of Fig. 4.11(a) and (b). The position of the peak in gate current at $V_c \approx 16$ V $\approx E_c \times d_i$ corresponds to the coercive field of $E_c = 60$MV/m of a P(VDF-TrFE) film with a thickness of $d_i = 0.3$ μm. The lack of the peak in the second cycle (C2) confirms the stability of the ferroelectric polarisation.[7,21,135] Due to the switching of the ferroelectric insulator from 'forward' towards 'reverse' bias at V_c the drain current exhibits two regions with different slopes on the forward sweep of the first cycle. Before the reversal of the ferroelectric polarisation ($V_{\mathrm{DS}} < V_c$) the increase of drain current is stronger than afterwards ($V_{\mathrm{DS}} > V_c$), indicating a further depletion of the surface and the concomitant reduction of conductivity at the surface. This behavior also confirms the results of the C-V measurements in the last section, which have shown a strong decrease of the MIS-device capacitance, i.e. caused by the depletion of the semiconductor, as the coercive field was exceeded under depletion voltages. On the back-sweep the drain voltage will not exhibit such a behavior, since all the ferroelectric domains have already been oriented. Also the second cycles follows in principle the slope of the back-sweep of the first one. Interestingly, although depleted, at the second cycle, the device shows a characteristic, similar to a device in accumulation (compare to Fig. 4.14), with linear region for low and saturation region for higher voltages. Such a behavior could be explained with the presence of negative, trapped charges at the insulator/semiconductor interface. The number of fixed charges seems to increase for each poling cycle leading to general increase in drain current from P1 towards P29.

When looking at the output characteristics at accumulation voltages in Fig. 4.12 (a), this above discussed change of slope of $I_{\mathrm{D}}(V_{\mathrm{DS}})$ at $V_{\mathrm{DS}} = V_c$ is not visible. For positive voltages the FeFET starts to accumulate holes as

depicted in Fig. 4.10 leading to an overall increased drain current, compared to the current under depletion voltages. The increase of $I_D(V_{DS})$ upon the poling cycles (P2) → (P30) is not as strong as in Fig. 4.11 (a) but also seems to saturate. Hence, in this measurement regime, the ferroelectric switching of the insulator has only a minor (or no) effect on the drain current. The dependence of each drain current curve is quadratic and can in principle be described by Equ. (2.30) for $V_t \approx 1$ V.[6]

The gate current in Fig. 4.12(b) clearly indicates a ferroelectric switching, although not as clear as for depletion voltages, since its superimposed with an increased DC current component.[78,79] Thus, it can be concluded that, the output characteristic starts to accumulate at voltages below V_c, before the ferroelectric polarisation was reversed. The fact that $I_D(V_{DS})$ does not reflect the ferroelectric switching may serve as a further confirmation for the existence of negative charges, which compensate the ferroelectric polarisation charge of the insulator.

The effect of the ferroelectric polarization on the accumulation and depletion behavior of the FeFET was also studied by means of the transfer characteristics given in Fig. 4.13(a). This set of measurement shows the source current as the FeFET is driven from depletion (V_{GS} = 40 V) towards accumulation (V_{GS} = −40 V) and subsequently back to depletion at drain voltages of 0 V and −5 V. The transfer characteristic is, furthermore, comparable with those presented by Naber *et al.* and other authors.[16,80] For the characteristics in Fig. 4.13(a) the drain voltage was, so to say, a parameter used to probe the change of conductivity of the interface as the gate voltage was varied between ±40 V. However, depending on the sign the drain voltage may reduce or increase the effective voltage between gate and drain contact. In order to reduce this effect, a relatively small drain voltage of −5 V was chosen, compared to the maximal gate voltage of ±40 V. The characteristics at 0 V is plotted to show the influence of the leakage current on the measurements. Fig. 4.13(b) shows the corresponding gate currents with the characteristic peaks caused by the ferroelectric switching.

Like the C-V characteristics of the MIS device in Fig. 4.4(b), also the transfer characteristics of the FeFET indicates a hysteresis in the current reading. As the gate voltage is driven from positive towards negative voltages, the measured source current starts to increase from $\approx 10^{-7}$ A at a depletion voltage of 5 V up to $\approx 10^{-4}$ A at −40 V. Although, during this voltage sweep, the reorientation of the ferroelectric domains, indicated by the peak in the gate current, does not start before 10 V a strong increase of source current up to this voltage has to be noticed already. At a gate voltage of −10 V the source current has increased to a value of $\approx 8 \times 10^{-6}$ A. This constitutes an increase of

[6] In this operation regime the drain contact (D) starts to act as source (for holes) and the source contact (S) has to be considered as drain.

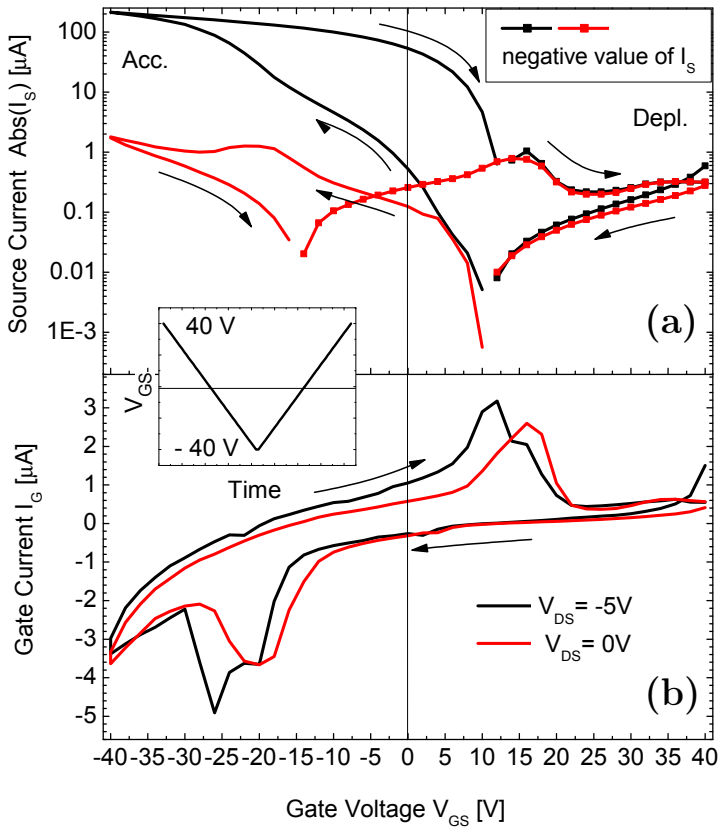

Figure 4.13: (a) Transfer characteristics for V_{DS} = 0 V and V_{DS} = −5 V as well as the (b) corresponding gate current. A strong increase of $I_{\mathrm{D}}(V_{\mathrm{GS}})$ for accumulation voltages is noticeable, although $V_{\mathrm{GS}} < V_c$. The kink in the logarithmic plot in Fig. (a) is due to the change of sign of V_{DS}. Negative values are marked with ■ symbols. The measurements start at V_{GS} = 40 V

current of almost two orders of magnitude and is (in this respect) comparable to the studied accumulation behavior of the MIS device. Further increase of gate voltage causes the reorientation of the ferroelectric domains at about 20 V leading to a slight increase of the slope of I_{DS}.

On the back sweep from accumulation towards depletion voltages, I_{DS} remains relatively high, until at 10 V the reversal of ferroelectric polarization induces the depletion of the device, associated with a strong decrease of the current reading. Hence, comparing the slope of the source current during the forward sweep, towards accumulation, with the back sweep, towards depletion, it appears obvious that the FeFET remains relatively stable in accumulation but lacks a stable depletion behavior. In that respect, the transfer characteristics of the FeFET shows the same accumulation and depletion behavior as the C-V curve of the MIS-device in Fig. 4.4(b) and may therefore serve as a further support of the idea of trapped negative charges and a stable ferroelectric polarisation.

Noticeable although is, that the transition from depletion towards accumulation in the C-V characteristics of the MIS device in Fig. 4.4(b) (page 58) appears much sharper and more shifted towards depletion voltages than it is in transfer characteristics in Fig. 4.13(a). Also Naber *et al.*[79] has found a gradual increase of drain current instead of a sharp transition from depletion towards accumulation at the coercive field and explained it with the dependency of the mobility on the charge carrier density on one side and with the depolarization of the insulator on the other side. Naber *et al.* also relate this behavior to a lack of remanent polarisation behavior observed in the C-V of a MIS-device. However, this is not attributed to depolarization, but as already mentioned due to the compensation of the remanent polarization of the insulator by fixed negative charges.[50]

Though, the explanation with the dependency of the charge carrier density on the mobility is to some extend equivalent to the findings in section 3.3.2.[51,126] There it was shown, that the charging of the surrounding electrode area through lateral currents can be related to a characteristic time, i.e. characteristic frequency. This time can be interpreted as the time needed by the charge carriers to travel in lateral direction and to accumulate at the area beyond the electrode. The characteristic time to charge the surrounding electrode area was longer than 10^2 sec for depletion voltages and was reduced to $\approx$ 10 sec for accumulation voltages. These calculated times may not fit exactly to the mobility measurements, since the channel geometry of the FeFET is certainly different from the assumed channel geometry of the MIS device. Furthermore, the characteristic times for accumulation and depletion are, in this work, changed by the variation of the spreading length, i.e. channel length L, and the effective bias voltage, but not by the modification of the channel mobility. However, a voltage change could in principle also be expressed by a change of channel mobility. Therefore the argumentation by Naber *et al.* is equivalent to the findings in section 3.3.2.

Hence, based on these results it appears reasonable to conclude that the gradual increase of the source current at depletion voltages can be explained with relatively long time needed by the charge carriers to accumulate at the interface of the channel. In accumulation the charge carrier are able to 'react' much more quickly therefore the source current reading is sharper at the transition from accumulation towards depletion.

After the above described measurement campaign, the hole mobilities were determined by means of Equ. (2.30) at the beginning of saturation, defined by $V_{DS} = V_{GS} - V_t$. The FeFET devices showed saturation mobilities typically in the range of 10^{-4} cm^2(sV)$^{-1}$...10^{-2} cm^2(sV)$^{-1}$, comparable to mobilities found by Zen *et al.*[143,144] and Estrada *et al.*[30] As an example Fig. 4.14 shows plots of output characteristics for gate voltages of of 0 V, −10 V, −20 V, −30 V and −40 V as well as a fit of Equ. (2.30) yielding a mobility and threshold voltage

of 2×10^{-3} cm^2(sV)$^{-1}$ and −0.5 V, respectively.

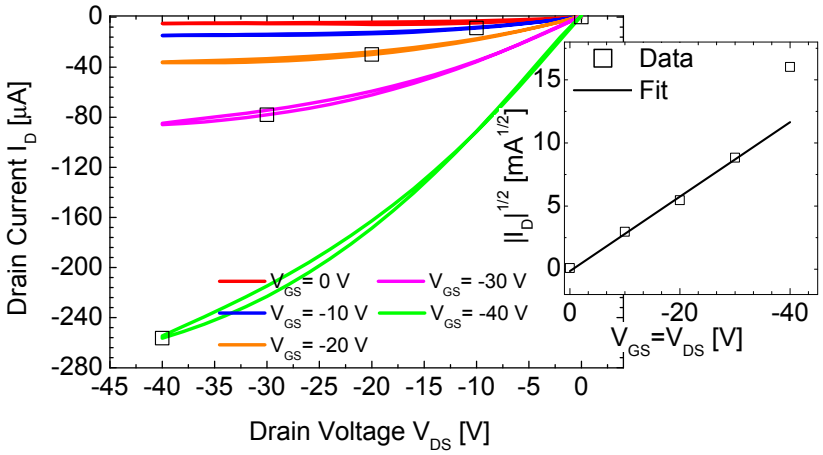

Figure 4.14: Output characteristics measured at gate voltages of 0 V, −10 V, −20 V, −30 V, −40 V. Plot of $\sqrt{|I_{DS}|}$ in the saturation regime (V_{DS} = V_{GS}). The fit by means of Equ. (2.30) yields a mobility and threshold voltage of 2×10^{-3} cm^2(sV)$^{-1}$ and −0.5 V, respectively. The fit was performed with $C_i' = 5.8 \times 10^{-4}$ F/m^2.

Conclusion

In conclusion the FeFET measurements confirm the previous results of the stability on the ferroelectric polarization and the presence of negative charges at the insulator-semiconductor interface. The output characteristics in Fig. 4.11(a) suggest a permanent trapping of negative charges at the interface during the first poling steps, leading to an increased drain current for negative drain voltages with increasing numbers of poling cycles. Transfer characterstics as well as the C-V curves of the MIS device (shown in Fig 4.4(b) on page 58) demonstrate a lack of stable depletion behavior. The effect of compensation of the remanent polarization by negative charges on the accumulation behavior of FeFET was confirmed by means of transfer and output characteristics.

4.5 Effect of stable Ferroelectric Polarization on Thermally Stimulated Current (TSC) measurements

In the previous sections 4.1, 4.2 and 4.3 the dielectric properties of MIS devices have been studied by measuring the capacitance as a function of voltage and frequency at a fixed temperature. Relaxation processes such as the MW process were characterized by its position in the capacitance spectra and its dependence on an applied bias. It is, however, also possible to study relaxation processes

by measuring DC currents as a function of temperature, known as thermally stimulated current (TSC). The section below presents, among other results, further evidence for the stability of the polarization under depletion voltages.

Introduction

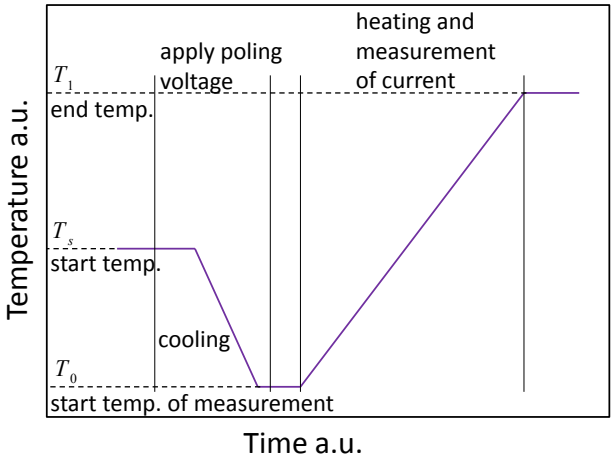

Figure 4.15: Standard TSC measurement with a poling phase starting at a temperature T_s and a measurement phase between the temperatures T_0 and T_1. The measurement of the TSC is taken at a constant heating rate with a short circuited sample.

The standard TSC measurement as shown in Fig. 4.15 starts with poling the sample at a temperature T_s. This poling voltage induces an electrical field causing molecular and charge polarization within the sample. The sample is then cooled under the applied field towards the temperature T_0. All polarization processes with an activation temperature above T_0 are therewith frozen in. When T_0 is reached the applied field, is removed and the sample is short circuited. After a short depolarization time, which allows for the relaxation of processes with an activation temperature below T_0, the actual TSC measurement starts. During this step the sample is heated at a constant rate from T_0 towards a target T_1 while the current is permanently measured. If the relaxation temperature of a process is reached, the drift of charges or the reorientation of molecular dipoles cause change of compensation charges at the electrodes and with that a peak in the current reading, which can be evaluated with Equ. 4.13.

The interpretation of these relaxation processes can be difficult, since current peaks may be caused by detrapping of charge carriers or by molecular reorientation. It is in principle also possible that both processes occur at the same time. Hence, it is always necessary to compare TSC data to other measurements such as for instance differential scanning calorimetry (DSC). One advantage, however, of TSC measurement is that the temperature dependence of the relaxation time can be inferred from a single measurement.

Thermally activated relaxation processes of poly(3-alkylthiophene)s (P3-AT) such as P3HT have been well studied[12–14,42,139,147] throughout the last

decades. From dynamic mechanical analysis (DMA) and DSC Chen *et al.*[12–14] have identified three main relaxations in P3HT, referred to as α, β and γ. The α- relaxation (or glass transition) from −12°C to 70°C, centered at 26°C, is attributed to twists in the main chains, formed by a chain of thiophene rings. The β- relaxation from −120°C to −20°C, centered at −26°C, refers to the motion of the hexyl side chains. Below −150°C all P3ATs show the γ-relaxation which is assigned to the motion of the methylene linkages of the side chains.

Zhao *et al.*[147] have shown that it is possible to distinguish between two crystallization processes in P3HT, a slow process and a fast process. The slow crystallization process starts at a relatively low crystallization temperature of around 40°C and shows a melting temperature which is always approximately 30°C above the crystallization temperature. The fast process lead to crystals with a nearly constant melting temperature of 173°C. It was further shown that for crystallizations above 140°C both melting temperatures coincided at 173°C.

Temperature dependent structural changes in PVDF and P(VDF-TrFE) are also well studied by dielectric and calorimetric measurements such as TSC, DSC and dielectric spectroscopy.[29,34,45,46,49,74,83,104,119,128,129,140] It was found by Sasabe *et al.*[107] that PVDF shows three relaxations. In the TSC measurements, the α_a-relaxation at around −30°C corresponds to the glass transition and is attributed to the micro-Brownian motion of the amorphous phase, the α_c-relaxation is assigned to molecular motions in the crystalline regions of α-PVDF and is found at 80°C. At temperatures of around −50°C and at frequencies between 100 Hz and 1 kHz the dielectric spectra reveal the β-relaxation attributed to local motions within the frozen main chains in the amorphous regions.[83,107] This relaxation however is low in magnitude compared to α_a and α_c and therefore difficult to detect in the dielectric spectra. As the temperature increases the β-relaxaion becomes indistinguishable from the α_a-relaxation in the dielectric spectra.[107|7]

TSC and DSC measurements of P(VDF-TrFE) with different molar fractions, performed by Teyssedre *et al.*,[128–130] showed two relaxations which refer to the glas transition between −50°C and −30°C as well as a relaxation associated to crystallites between 20°C and 50°C. Referring to Teyssedre *et al.*[129,130] this temperature however would only be related to crystal domains in so far as it has been ascribed to reorganizations at the crystallites surface rather than in the bulk of crystallites. Another explanation concerning the relaxation between 20°C and 50°C has been but forward by Rollik *et al.*,[105] who studied stretched PVDF films by means of different poling schemes. He assigns this relaxation to

[7]The naming of the relaxations is ambiguous. The relaxation related to the glass transition is in some cases also referred to as β-relaxation.[49] In those cases the relaxation related to chain movements in the crystallites are labeled as α-relaxation.

the accumulation of charges at the amorphous-crystalline interface and referes to it as Maxwell-Wagner effect. Although both authors have different explanations for the origin of the relaxation, it has to be noted that both explanations of Rollik and Teyssedre are based on processes at the interface of crystallites.

The Curie temperature of P(VDF-TrFE) is about 120°C (for 73/27 $mol\%$ of VDF/TrFE) and results in a large peak in DSC as well as TSC measurements.[31,33]

A mathematical description of a TSC current density of a temperature dependent Debye process can be found as[1,11]

$$J(T) = \frac{\mathrm{d}P\left(T(t)\right)}{\mathrm{d}t} = \frac{\mathrm{d}P(T)}{\mathrm{d}T}\frac{\mathrm{d}T}{\mathrm{d}t} = \frac{\mathrm{d}P(T)}{s\mathrm{d}T} = -\frac{P(T)}{\tau(T)}. \tag{4.12}$$

The polarisation stored during the first cooling step of the TSC is given with P. At the second step the temperature is increased at a rate $\mathrm{d}T/\mathrm{d}t = s^{-1}$. The relaxation process manifest its self as peak in the current during the heating at a rate s^{-1}. Its position T_p is given by the condition $\mathrm{d}\tau(T)/\mathrm{d}T = -s$.

From a well separated peak in the current reading the relaxation time can be inferred with

$$\tau(T) = \frac{s}{J(T)}\int_T^{T_b} J(T')\mathrm{d}T' \quad \text{for} \quad T_a \le T \le T_b. \tag{4.13}$$

The temperatures T_a and T_b have to be chosen such that the integration is taken over the entire current peak. Once the relaxation time $\tau(T)$ is know, the activation energy of the process, E_a, can be determined by a linear fit of $\ln(\tau)$ over $1/T$.

The temperature dependence of the relaxation time above the glass temperature is often given by the Arrhenius law

$$\tau(T) = \tau_0 \exp(E_a/kT) \tag{4.14}$$

with τ_0, and k as exponential pre-factor (or reciprocal frequency factor) and the Boltzmann's constant, respectively.[44]

The relaxation time of the α process, related to the glass transition can be described with the Vogel Fulcher law

$$\tau(T) = \tau_0^{VF} \exp(B/k(T - T_0^{\mathrm{VF}})) \tag{4.15}$$

were τ_0^{VF}, B and T_0^{VF} represent the pre-exponential factor, the apparent activation energy and a characteristic temperature, respectively. This equation reflects, so to say, the increase of viscosity of the amorphous polymer as the temperature is decreased towards the glass transition temperature.[8]

[8]Definition: The glass temperature is related to the temperature where the relaxation time, described by the Vogel Fulcher law, approaches 1000 s.[23]

Experimental & Discussion

The Fig. 4.16 shows several TSC measurements of a MIS device with negative and positive poling voltages of ±30 V. The TSC measurements were performed on the same devices as used for the determination of the interface trap density in section 4.3. The negative and positive contact was made to the bottom and top electrode, respectively.

First a standard TSC measurement was performed as shown with the purple curves in Fig. 4.16(a) and (b). Before the TSC measurement the sample was subjected to a pre-poling where bias voltages of ±30 V was alternated 5 times to ensure that all ferroelectric domains are fully poled.[25,28] Each voltage step of the pre-poling was applied for 1 min. Directly after the pre-poling the TSC measurement started with the poling at either +30 V or −30 V for 4 min at a temperature of 20°C followed by the cooling of the sample. When the temperature of T_0 = −80°C was reached the poling voltage was removed, the device was short circuited and kept at this temperature for about 4 min before the sample was heated at a rate of 7 K/min towards T_1 = 100°C. The black curves in Fig. 4.16(a) and (b) show the background current TSC measurements, attributed to pyroelectric and conduction contributions. They were measured right after the standard TSC measurement and followed the same measurement procedure, however, without any application of voltage.

The standard TSC measurement shows two clear relaxation processes centered at −35°C and 25°C, which changed their polarization but not the position upon the poling direction. Above 50°C another relaxation is found at 60°C which, contrary to the other two peaks, is only clearly visible when the device is poled to 30 V. When poled to −30 V the peak shifts to higher temperatures of around 80°C.[31]

In order to separate those peaks more clearly a partial heating procedure as depicted in Fig. 4.17 was used. In its course the sample was pre-poled and poled in the same way as for the standard TSC procedure (T_s = 20°C , T_0 = −80°C) however followed by three heating steps (T_1 = −20°C, T_2 = 50°C, T_3 = 100°C) at a rate of 7 K/min each followed by a subsequent cooling of the sample. The three resulting TSC curves fit well to the standard TSC measurements which proves the reproducibility of the relaxation processes.

These three measurements were corrected for the contribution of the background conduction current and by means of Equ. (4.13) further used for the calculation of the respective relaxation times, given as Bucci plot in Fig. 4.18(a) for positive poling and (b) negative poling. The calculated $\tau(T)$ for the process around −35°C in Fig. 4.18(a) and (b) does not show a clear Arrhenius behavior and shows a different slope for temperatures below −50°C ($4.510^{-3}\mathrm{K}^{-1}$). The change in slope might be due to an additional process at about −70°C, visible as shoulder in the low-temperature rise. The position of the peak in the TSC

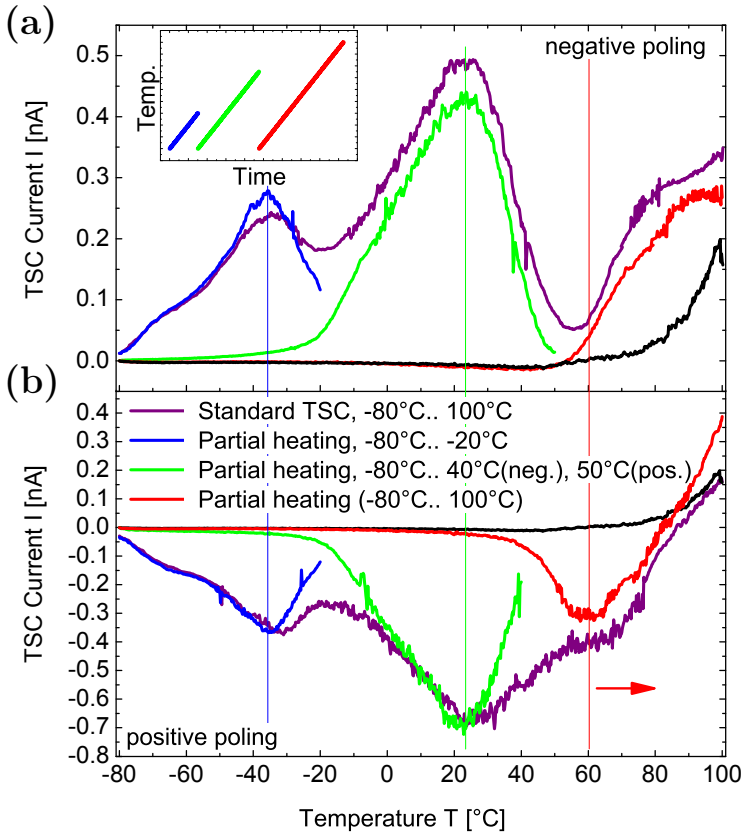

Figure 4.16: TSC measurements of the MIS devcie with standard procedure (purple) as given in Fig. 4.15 for (a) negative (depeltion) and (b) positive (accumulation) voltages. The blue green and red curves are obtained by a partial heating procedure as depicted in Fig. 4.17. For both types of TSC measurements a heating rate of 7 K/min as well as the same poling and pre-poling parameters were used. Inset shows heating scheme of partial heating procedure (i.e. peak clearing).

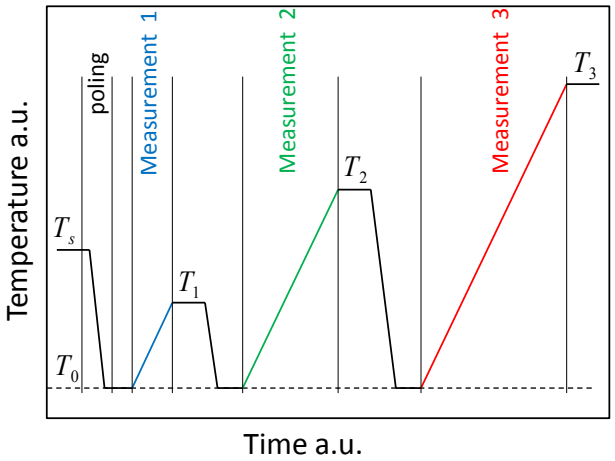

Figure 4.17: TSC measurement with three partial heating cycles as used in Fig. 4.16. Each starting at T_0 = −80°C and and ending at T_1 = −20°C, T_2 = 50°C and T_3 = 100°C. Poling started at T_s = 20°C. Each measurement of the TSC is taken at a the same constant heating rate of 7 K/min with a short circuited sample.

curve corresponds very well to the glass transition of P(VDF-TrFE).[57,69,107,129]

Unfortunately, not enough data points are available in the high temperature part of this process, therefore a fitting by the Vogel-Fulcher law in this temperature range can not be performed. The lack of a clear Vogel-Fulcher behavior could also be explained by the presence of another relaxation process that assists the glass transition. It could be that the adjacent relaxation at around 20°C is not completely separated by the partial heating procedure. However, Since P3HT does not show relaxation processes in this temperature range, the peak has to be mainly related to the glass transition of P(VDF-TrFE).

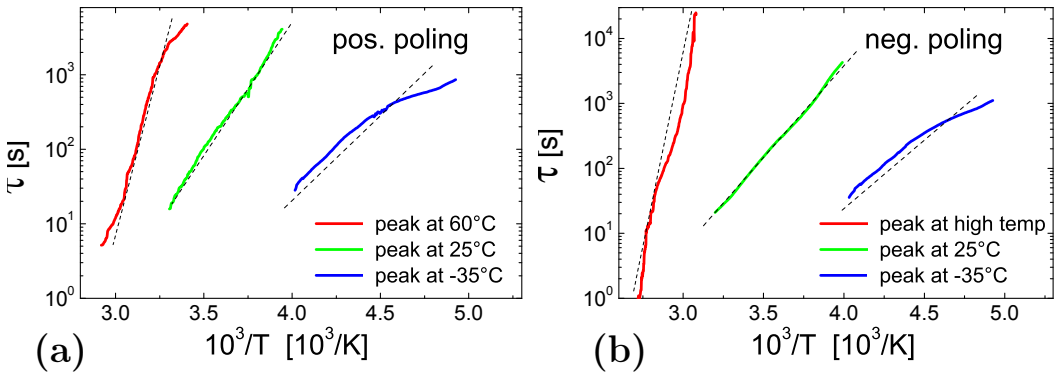

Figure 4.18: Plots of the relaxation times as calculated from the peak at −35°C, 25°C and above 50°C after poling with (a) positive and (b) negative voltage. The dotted lines are guides to the eye.

The TSC peak at 25°C is also identified as a relaxation process of the P(VDF-TrFE). In principle this peak could have also been associated with the glass transition of P3HT, usually termed as α-relaxation, which takes place at around the same temperature.[42,147] However, the corresponding Bucci plots in Fig. 4.18(a) and (b) yield an almost linear, i.e. Arrhenius like, behavior for the relaxation time and should therefore not relate to a glass transition. Hence, it is concluded that this process is dominated by relaxations within the P(VDF-TrFE) layer.

Relaxations of P(VDF-TrFE) for temperatures above 0°C have been discussed for instance by Menegotto *et al.*,[69] Teyssedre *et al.*[130] Also Rollik *et al.*[105] has performed TSC studies on stretched PVDF under the application of different poling schemes. Using the interpretation of Teyssedre *et al.* and Menegotto *et al.* the measured relaxation at 25°C could be related to conformational reorganization at the crystallites surface. From their point of view this α-relaxation, as they call it, can be found in α- as well as in β-P(VDF-TrFE) and is therefore not an intrinsic property of a specific crystalline conformation. Another interpretation for the TSC peak at 25°C is made by Rollik *et al.*,[105] who relates this relaxation to a Maxwell-Wagner effect caused by the trapping of charges at the amorphous- crystalline interface (α- PVDF) as well as interfaces of ferroelectric crystallites (β- PVDF). It is therefore possible that the

relaxation in the TSC measurements found by Teyssedre *et al.* and Menegotto *et al.* is related to the same phenomenon discussed by Rollik *et al.* On the other hand it can not be excluded that there is such a α-relaxation yet it is not sure that the TSC peak is associated with it.

The poling procedure used by Rollik *et al.* is very similar to the one used in this study. Hence, it appears plausible that the measured TSC peak at 25°C in Fig. 4.17(a) and (b) is due to space charges as described by Rollik *et al.* This would also fit to the results found by Eisenmenger *et al.*[25–28], who discussed the importance of charge trapping for the stabilization of the ferroelectric polarization in PVDF. Thus, the peaks may prove charge injection into insulator as well as persistent trapping of the charges up to the temperature of 25°C for both polarization directions. However, they may also yield evidence for the stability of the ferroelectric polarization. An argument for this interpretation could be that the sample was cooled under a field above the coercive field of the P(VDF-TrFE). Hence, the space charges in this case may also be trapped at the interface of ferroelectric domains.[105] It is then reasonable to assume, that if ferroelectric domains were depolarized under depletion, as suggested by Naber *et al.*[80], that this would cause a release of the trapped space charges and cause an additional peak in TSC current or shift of the existing peak during the heating step. However, the TSC look very similar for both poling directions, i.e. for accumulation and depletion, and does not show any additional or shifted peaks when the device was poled with a negative (depletion) voltage. In conjunction with the findings in the section 4.2 this result constitutes a strong argument for the stability of the ferroelectric polarization.

Looking further at the high temperature region, the separation with the partial heating procedure makes clear that the relaxation above 50°C depends on the poling voltage. This region of the TSC spectra was also studied by Neto *et al.*[87] and Faria *et al.*[31,87] who have found a peak which was shifted to higher temperatures with increasing TrFE content. Both authors concluded, that this relaxation is related to a ferroelectric to paraelectric transition. The involvement of space charges was also considered as possible. A change of VDF/TrFE ratio will result in a change of number of boundary regions as discussed by Furukawa *et al.*[34]

It can therefore be theorized, that this relaxation process is confined to the P3HT/P(VDF-TrFE) interface rather than to the insulator bulk. The bottom contact of the device was connected to the ground. Therefore a positive poling voltage would lead to an injection of large numbers of positive charges into the P3HT layer and a concomitant accumulation of positive charges at the interface. Those charges might then get trapped at the interface and released upon the heating as result of structural reorganisation of crystallite boundaries located at the interface leading to a peak in the TSC plot at around 60°C.

Thus following this train of thought, a reversal of the poling voltage could

also lead to trapping of negative charges at the interface. Although P3HT is known as a p-type semiconductor, evidence has been found about the presence of negative charges.[18] Those negative charges would then be released during the heating. Hence, a shift of the relaxation peak towards higher temperatures for negative poling voltages could indicate deeper trap sites for negative charge carriers than for positive charges.

The exact origin of this peak above 50°C and its behavior upon the poling voltage can not be clearly inferred from this set of measurement. Also, the calculated relaxation times allow no further conclusions. Explanations therefore remain speculative. The TSC measurement only measures a macroscopic, global change of compensation charge upon heating. It is therefore difficult to draw conclusions about local microscopic processes from this TSC measurement. The high temperature behavior strongly suggests, however, the involvement of mobile charge carriers, i.e. space charges, in this relaxation process.

Conclusion

In conclusion it was shown that the relaxations at −35°C and 25°C are associated to the glass transition and an interface polarisation effect at crystallites on the boundaries of the amorphous phase of P(VDF-TrFE), respectively. The position as well as the magnitude of the interface polarisation peak is independent of the poling direction. This might serve as a further argument for the stability of the polarization under depletion voltages. The exact origin of the relaxation above 50°C could not be inferred from this measurement, however, it could be related to charge trapping at the semiconductor/insulator interface.

5 Final Conclusion and Outlook

The above presented study was concerned with the lack of stable depletion behavior of MIS structures and with the related charge trapping processes at the insulator/semiconductor interface. In this context, MIS devices were subjected to I-V, C-V, C-f as well as TSC measurements and FeFETs were studied by means of output and transfer characteristics. Two main results emerge from these measurements:

- the stability of the ferroelectric polarization of the insulator and
- the presence of negative compensation charges as well as fast interface traps at the insulator/semiconductor interface.

The C-V and FET characteristics clearly suggest that the instable depletion behavior has to be explained by the presence of fixed compensation charges. The stability of the ferroelectric polarization in accumulation and in depletion mode was confirmed by C-V, I-V, TSC as well as the transistor measurements.

By determining the position and height of the MW peak in capacitance spectra, it was demonstrated in section 4.1 that the device started to deplete for voltages above the coercive voltage (given by $E_c \times d_i$), however, it did not remain in a stable depletion state. Based on C-V and I-V characteristics measured with an unipolar/bipolar voltage pattern, it was then demonstrated in section 4.2 that, contrary to previous suggestions,[77,80,81] the ferroelectric polarization in P(VDF-TrFE)/P3HT MIS devices remains stable both in accumulation and depletion mode. Therefore, depolarization of the insulator can no longer serve as an explanation for the apparent lack of stable depletion behavior.

It was further theorised that electron transfer from the P3HT depletion region into insulator-related trap states at or near the insulator/semiconductor interface could lead to compensation of ferroelectric polarization. The high density of fixed electrons is sufficient to even overcompensate the ferroelectric polarization. This leads to the suggestion that the electrons are deeply trapped at the surface of crystallites located near the interface to the semiconductor. The results in section 4.3 indicated the presence of a second type of traps, known as fast interface traps. These trap states were clearly identified and evaluated by their characteristic peak in the loss-voltage curves by means of

the conductance method, developed by Nicollian and Goetzberger.[96,113] This method revealed a distribution of interface trap sites of around 10^{11} $(\mathrm{eVcm}^2)^{-1}$, which is in the same order of magnitude as found for other organic P3HT based MIS systems.[2,126] This evaluation method became applicable after the removal of the influences of the ferroelectric switching from the C-V plots by means of unipolar/bipolar voltage pattern.

The measurements on FeFETs in section 4.4 confirm previous results on the stability of the ferroelectric polarization and the presence of fixed negative charges at the insulator-semiconductor interface. Furthermore the output characteristics in Fig. 4.11(a) suggest permanent trapping of negative charges at the interface during the first poling steps, leading to an increased drain current for negative drain voltages with an increasing number of poling cycles.

The TSC measurements in section 4.5 yield further evidence for the stability of the ferroelectric polarization. Here, the position as well as the magnitude of the interface-polarisation peak at 25°C is independent of the poling direction and therefore indicates the stability of the polarization in accumulation as well as in depletion. The exact origin of the relaxation above 50°C could not be determined from the measurement, however, it could be related to a charge trapping process at the semiconductor/insulator interface.

TSC measurements might also serve as motivation for further TSC studies in combination with C-V measurements. Since C-V curves can provide clear evidence about the number and polarity of charges, the combination with a TSC measurement can give information about whether or not charges have been removed from trap sites at a given temperature. One idea is to perform a C-V measurement before and after a TSC measurement. The presence of fixed interface charges can be measured with a C-V curve before the TSC measurement. When fixed charges are removed upon heating it should, in principle, be possible to see this phenomenon in the TSC current, as well as in subsequent C-V curves.

The above findings suggest the improvement of the interface between P3HT and P(VDF-TrFE) to enhance the stability of these organic MIS devices. The inclusion of an electron blocking layer at the interface could be one option. Such a layer should prevent the effect of charge trapping and lead to an increased data retention time for the memory device. Blocking layers and surface treatment have been successfully implemented on silicon oxide surfaces and led to increased performance due to the reduction of trap sites at the interface.[18,146] It is therefore reasonable to conclude that similar optimization of the P(VDF-TrFE) interface might also lead to a reduction of trap sites, increase the performance of the MIS devices and consequently improve the data retention time of organic FeFETs.

Appendix

Modeling C-V Spectra

A numerical description of the C-V behavior of MIS structures with a ferroelectric gate insulator is given in[71]. The set of equations, required to describe charging of such structures can be derived as follows.

Generally, the displacement vector of a dielectric material, at an applied field E_i, is given by

$$\vec{D} = \varepsilon_0 \vec{E}_i + \vec{P}^* \tag{5.1}$$

with $\vec{P}^*$ as polarization, caused by molecular polarization or charge displacement. In ferroelectric materials the total polarisation $\vec{P}^*$ can be written as a sum of an homogeneous, isotropic dielectric contribution $\varepsilon_0 \varepsilon \vec{E}_i$ and a contribution $\vec{P}(\vec{E}_i)$ arising from the molecular dipoles. Thus, the polarisation $\vec{P}^*$ yields

$$\vec{P}^* = \varepsilon_0 \chi \vec{E}_i + \vec{P}, \text{ with } \chi = \varepsilon_i - 1 \tag{5.2}$$

$$\vec{P}^* = \varepsilon_0 \varepsilon_i \vec{E}_i - \varepsilon_0 \vec{E}_i + \vec{P}(\vec{E}_i) \tag{5.3}$$

$$. \tag{5.4}$$

With that, the electrical displacement for ferroelectric materials is written as

$$\vec{D} = \varepsilon_0 \varepsilon_i \vec{E}_i + \vec{P}(\vec{E}_i). \tag{5.5}$$

Gauss law relates the electrical displacement vector $\vec{D}$ to the charge density ρ. Hence, Gauss yields a relation between the applied field $\vec{E}_i$ and the accumulated charges on the dielectric material. The orientational polarisation of the dipoles is anti parallel to the applied field E_i, therefore, for this direction $\vec{P}(\vec{E}_i) \to -P(E_i)$. The one dimensional case then yields

$$\rho = \nabla \vec{D} \tag{5.6}$$

$$\rho = \frac{\mathrm{d}}{\mathrm{d}x} \varepsilon_0 \varepsilon_i E_i - \frac{\mathrm{d}}{\mathrm{d}x} P(E_i) \tag{5.7}$$

$$\mathrm{d}x\rho = \varepsilon_0 \varepsilon_i \mathrm{d}E_i - \mathrm{d}P(E_i) \tag{5.8}$$

$$\int_0^d \rho \mathrm{d}x = \varepsilon_0 \varepsilon_i \int_0^d \mathrm{E_i(d)} E_i(d) - \int_0^{P(E_i(d))} \mathrm{d}P(E_i(d)) P(E_i(d)) \tag{5.9}$$

$$\sigma = \varepsilon_0 \varepsilon_i E_i - P(E_i). \tag{5.10}$$

The integration over a given film thickness d yields the charge per unit area σ, the applied field E and the orientational polarisation $P(E_i)$. Utilizing $E = -\nabla \psi = \frac{\Delta V_i}{\Delta d}$ it follows that

$$\sigma = -\varepsilon_0 \varepsilon_i \frac{\Delta V}{\Delta d} - P(E_i). \tag{5.11}$$

$$\Delta V_i = -\sigma \frac{\Delta d_i}{\varepsilon_0 \varepsilon_i} - P(E_i) \frac{\Delta d_i}{\varepsilon_0 \varepsilon_i}. \tag{5.12}$$

This equation describes the polarisation of a single ferroelectric layer and implies that the ferroelectric polarisation has to satisfy the condition

$$E_i = -\frac{\sigma}{\varepsilon_0\varepsilon_i} - \frac{P(E_i)}{\varepsilon_0\varepsilon_i} \tag{5.13}$$

$$E_i = -\frac{\sigma + P(E_i)}{\varepsilon_0\varepsilon_i}. \tag{5.14}$$

The equation is self consistent, since the polarisation $P(E_i)$ depends on the electric field E_i. The charge per unit area σ has to be interpreted as the charge density on the ferroelectric layer, which has to be supplied by the signal source, that is to say by the electrodes.

The further considerations shall be made for a multilayer system of insulators, each described by its own dielectric constant $\varepsilon_{1,2,..}$ and film thickness $d_{1,2,..}$. For a stack of insulators the voltage drop V_i over this entire multilayer system can be written as

$$E_i = \nabla V \tag{5.15}$$

$$E_i = \frac{\mathrm{d}V}{\mathrm{d}d} \quad \longrightarrow \tag{5.16}$$

$$\int \mathrm{d}V = \int E_1 \mathrm{d}d \tag{5.17}$$

$$V_i = E_1 d_1 + E_2 d_2 + ... = V_1 + V_2 + ... \tag{5.18}$$

Utilizing the aboves result and assuming that only layer '1' (V_1, ε_1) as a ferroelectric contribution, $P(E_1)$, gives

$$V_i = E_1 d_1 + E_2 d_2 + ... = V_1 + V_2 + ... \tag{5.19}$$

$$V_i = \left(-\sigma\frac{d_1}{\varepsilon_0\varepsilon_1} - P(E_1)\frac{d_1}{\varepsilon_0\varepsilon_1}\right) + \left(-\sigma\frac{d_2}{\varepsilon_0\varepsilon_2}\right) + ... \tag{5.20}$$

$$V_i = -\sigma\left(\frac{d_1}{\varepsilon_0\varepsilon_1} + \frac{d_2}{\varepsilon_0\varepsilon_2} + ...\right) - P(E_1)\frac{d_1}{\varepsilon_0\varepsilon_1} \tag{5.21}$$

In the last step it was used, that the charge density $\sigma = \mathrm{d}x\rho = D = \varepsilon_0\varepsilon E$ is the same at each interfaces due to the continuous boundary condition

$$D = D_1 = D_2 = ... \quad \longrightarrow \tag{5.22}$$

$$\sigma = \sigma_1 = \sigma_2 = ... \tag{5.23}$$

However, for a MIS multilayer system with a semi conducting layer in series with the insulating ferroelectric layer the applied voltage on the MIS is given as the sum

$$V_{MIS} = V_i + V_s. \tag{5.24}$$

This expression in conjunction with equation (5.21) can be rearranged to

$$V_i = V_{MIS} - V_s = -\sigma\left(\frac{d_1}{\varepsilon_0\varepsilon_1} + \frac{d_2}{\varepsilon_0\varepsilon_2} + ...\right) - P(E_1)\frac{d_1}{\varepsilon_0\varepsilon_1} \tag{5.25}$$

$$V_{MIS} = V_s - \sigma\left(\frac{d_1}{\varepsilon_0\varepsilon_1} + \frac{d_2}{\varepsilon_0\varepsilon_2} + ...\right) - P(E_1)\frac{d_1}{\varepsilon_0\varepsilon_1}. \tag{5.26}$$

Any work function differences or additional trapped charges within the MIS could be modeled by adding the corresponding potential. However, at the moment those terms will not be considered.

The semiconductor is supposed to have an ohmic contact, through which charges can be induced. V_s is usually referred to as the semiconductors surface potential. The semiconductors charge density depends on the field V_s, hence $\sigma = \sigma(V_s)$ and is theoretically given by

$$\sigma(V_s) = -\mathrm{SIGN(V_s)}\sqrt{2}\left(\frac{\varepsilon_0\varepsilon_\mathrm{s}}{\beta \mathrm{L_b}}\right)\left[\left(\mathrm{e}^{-\beta \mathrm{V_s}} - \beta \mathrm{V_s} - 1\right) + \left(\frac{\mathrm{n_i}}{\mathrm{N_a}}\right)\left(\mathrm{e}^{\beta \mathrm{V_s}} - \beta \mathrm{V_s} - 1\right)\right]^{1/2}. \tag{5.27}$$

n_i is the intrinsic charge carrier concentration, the doping density and the Debye length is given by N_a and $L_b = \sqrt{\varepsilon_0\varepsilon_s/\beta q N_a}$ respectively. The above equations (5.26),(5.14) and (5.27) give a complete description of the polarisation and fields of a MIS. The applied voltage V_{MIS} relates to the charge density $\sigma(V_s)$ and the ferroelectric polarisation trough Equ. (5.26). The field E_1, responsible for the polarisation of the ferroelectric layer is given by (with $E_i = E_1$ and $\sigma(V_s) = \sigma$) Equ. (5.14).

This set of Equ. (5.26),(5.14) as well as (5.27) is nonlinear and has to be solved numerically. The nonlinearity is due to the dependence of the ferroelectric polarisation on field E_i as described by the self-consistent Equ. (5.14). Hence, the actual polarisation not only depends on the applied field but also on its 'history'. The polarisation $P(E)$ is given by theory and can be found elsewhere[71]. $P(E)$ yields the characteristic hysteresis loop and is defined by the differential equation,

$$\frac{\mathrm{d}P}{\mathrm{d}E} = \Gamma\frac{\mathrm{d}P_{sat}}{\mathrm{d}E} \quad \text{with} \tag{5.28}$$

$$\Gamma = 1 - \tanh\left[\sqrt{\frac{P - P_{sat}}{\xi P_s - P}}\right] \quad \text{and} \tag{5.29}$$

$$P^+_{sat}(E) = P_s \tanh\left[\frac{(E - E_c)}{2\delta}\right] \quad \text{where} \tag{5.30}$$

$$\delta = E_c\left[\ln\left(\frac{1 + P_r/P_s}{1 - P_r/P_s}\right)\right]^{-1}. \tag{5.31}$$

The negative-going branch of the saturated hysteresis loop P^-_{sat} is given by $P^-_{sat}(E) = -P^+_{sat}(-E)$ and $\xi = +1$ if $\mathrm{d}E/\mathrm{d}t > 0$ and $\xi = +1$ if $\mathrm{d}E/\mathrm{d}t < 0$. P_r, P_s

and E_c are the remanent and spontaneous polarisation and the coercive field, respectively.

A numerical solution of the above problem has been suggested by Miller *et al.*[71] and shall be roughly explained at this point. Considering a finite step width, the derivative $\mathrm{d}P(E)/\mathrm{d}E$ yields

$$\Delta P(E) = \frac{\mathrm{d}P(E)}{\mathrm{d}E}\Delta E \quad \Longrightarrow \tag{5.32}$$

$$P(E_m) - P(E_{m-1}) = \left.\frac{\mathrm{d}P(E)}{\mathrm{d}E}\right|_{E_{m-1}} (E_m - E_{m-1}) \tag{5.33}$$

$$P(E_m) = P(E_{m-1}) + \left.\frac{\mathrm{d}P(E)}{\mathrm{d}E}\right|_{E_{m-1}} (E_m - E_{m-1})\,. \tag{5.34}$$

Index m has been introduced for the summation or integration increment. In conjunction with the field E_m given by equation 5.14, E_m can be substituted and the entire expression rearranged. Hence, the polarisation becomes

$$P(E_m) = \frac{P(E_{m-1}) - \{[\sigma(V_s)/\varepsilon_0\varepsilon_i] + E_{m-1}\} \left.\frac{\mathrm{d}P(E)}{\mathrm{d}E}\right|_{E_{m-1}}}{1 + \frac{1}{\varepsilon_0\varepsilon_i} \left.\frac{\mathrm{d}P(E)}{\mathrm{d}E}\right|_{E_{m-1}}}. \tag{5.35}$$

In order to start the computation, it is first necessary to define the computation parameters which are given by the used materials and the device geometry. These include for instance P_r, P_s, E_c, N_a, μ, T and so on. With these parameters the initial values V^0_{MIS} and $P(E_0) = P_0$ have to be chosen in such a way to ensure that the polarisation lies within the saturated hysteresis loop. With these values the equations (5.26) and (5.27) may then be solved to obtain V^0_s and $\sigma(V^0_s)$. Once, P_0 and $\sigma(V^0_s)$ are known, the field E_0 as well as $\mathrm{d}P/\mathrm{d}E$ can be calculated using equation 5.14 and 5.28, respectively.

The variable of this computation algorithm is the surface potential of the semiconductor V^m_s. Hence, each integration step $m > 0$ starts with choosing $V^m_s = V^{m-1}_s + \Delta V_s$. The charge density $\sigma(V^m_s)$, the polarisation$P(E_m) = P_m$, the applied voltage V^m_{MIS} and the field E_m is then successively calculated from it. Schematically the calculation of the mth value is done as follows:

$$\begin{array}{ll} V_s & \\ \downarrow & \text{Equ. (5.27)} \\ \sigma(V_s) & \\ \downarrow & \text{Equ. (5.35), with } E_{m-1}, P_{m-1} \\ P(E_m) & \\ \downarrow & \text{Equ. (5.26)} \\ V_{MIS} & \\ \downarrow & \text{Equ. (5.14)} \\ E_m & \end{array}$$

Once the calculation is accomplished all values are known and the polarisation can be plotted (for instance) as a function E or V_{MIS}. With the numerically obtained data, σ, V_s, V_{MIS} it is feasible to compute further quantities such as the capacitance of the interface

$$C_D = \mathrm{d}\sigma/\mathrm{d}V_s, \tag{5.36}$$

the capacitance of the ferroelectric insulator

$$C_i = \varepsilon_0\varepsilon_r\frac{A}{d} + A\frac{\mathrm{d}P}{\mathrm{d}V_i} \tag{5.37}$$

and with that the capacitance voltage characteristic of the MIS device

$$C_{MIS}(V_{MIS}) = \frac{C_iC_D}{C_i + C_D}. \tag{5.38}$$

List of Symbols

Symbol	Description
A	Electrode area
B	Activation energy of Volgel Fulcher law
β	Reciprocal thermal potential ($\equiv q/KT$)
C_d	Capacitance of depletion zone
C_i	Insulator capacitance
C_i'	Insulator capacitance per unit area
C_m'	Measured capacitance per unit area
C_{MIS}	Capacitance of MIS structure
C_p	Capacitance of IT equivalent circuit
d_d	Depletion zone width
d_i	Insulator film thickness
d_s	Semiconductor film thickness
E	Electric field
E_a	Activation energy of Arrhenius law
ε_i	Permittivity of insulator
ε_s	Permittivity of semiconductor
ε_0	Vacuum permittivity
f	Frequency
G_{MIS}	Conductance of MIS structure
G_p	Conductance of interface trap (IT) equivalent circuit
I_{S}	Measured source current
I_{D}	Measured drain current
I_{DS}	Drain-source current
I_{G}	Measured gate current
I_{GS}	Gate-source current
J_m	Measured current density
k	Boltzmann constant
L	Channel length
M_n	Number average molecular weight
M_w	Weight average molecular weight
μ	Drift mobility
μ_b	Semiconductor bulk mobility
μ_{ch}	Semiconductor channel mobility

Symbol	Description
N_{ss}	IT density
ω	Angular frequency $2\pi f$
$P(E)$	Polarization charge density (= Q_p)
V_s	Semiconductor surface potential with respect to bulk
Q'_p	Polarization charge density (= $P(E)$)
Q_s	Number of semiconductor space charges (= $\sigma \times A$)
Q'_{T}	Interface trapped charge density
R_{el}	Contact resistance
R_i	Insulator resistance
R_{lf}	Low frequency capacitance of MIS structure
R_s	Semiconductor resistance
ρ_s	Semiconductor resistivity
σ	Semiconductor space charge density (= Q_s/A)
t	Time
T	Temperature
T_0	Start temperature of TSC measurement
T_0^{VF}	Characteristic temperature of Vogel Fulcher law
$T_{1,2,3}$	End temperatures of TSC measurment
T_s	Poling temperature of TSC measurement
τ	Characteristic relaxation time
$\tau_0,\ \tau_0^{\mathrm{VF}}$	Pre-exponential factors
$V(x)$	Potential between source and drain at position x
V_{FB}	Flatband voltage
V_{acc}	Accumulation voltage
V_{depl}	Depletion voltage
V_{DS}	Gate-source voltage
V_g	Gate voltage
V_{GS}	Gate-source voltage
V_t	Threshold voltage
W	Channel width
Z_{MIS}	Impedance of MIS structure

Curriculum Vitae

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Education and Qualifications

01.01.2008 - Present	Member of research staff at the University of Potsdam with studies for a PhD degree under supervision of Prof. R. Gerhard
01.10.2001 - 01.11.2007	Study of physics at the University of Potsdam (with Diploma Degree, made at group of Prof. A. Köhler)
01.10.2003 - 30.06.2004	Study of physics at the University of Southampton (two semester)
01.09.1998 - 07.07.2001	Secondary school Abitur-graduation through evening school in Potsdam (during employment, see below)
01.09.1993 - 30.01.1997	State Recognized Apprenticeship as Industrial Mechanic (specialization as flight engine mechanic) at MTU Aero Engines (Motoren- und Turbinen-Union) in Ludwigsfelde

Employment and Civil Service

02.11.2000 - 30.09.2001	Civil service at the Office for Environment and Nature Conservation in Potsdam
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01.01.2006 - 01.11.2007	Preparation and studies of organic semiconductor based devices, setup of light absorption and emission experiment at the Experimental Physics Group of Prof. A. Köhler
01.07. - 30.09.2004	Programming of numerical solutions of X-Ray diffraction on a 2-D super lattice structure at the Structural Analysis Group of Prof. U. Pietsch
01.07. - 30.08.2002	Programming and numerical calculation of charge transport and trapping in organic semiconductors at the Soft Matter Group of Prof. D. Neher

Teaching and Supervising

Supervising Skills	Participated in DAAD Rise exchange Program 2008 & 2010 as supervisor of exchange students, supervisor of a student assistant and mentor of his research internship
Teaching Skills	Leader of 5 weekly tutorials (2008-2010), participated in proj.: Improving Minor Subject Studies (SEPHA - Didaktische Konzepte für die strukturierte Studieneingangsphase)

Conference Contributions & Publications

Conference Contributions

10.4. - 14.4.2011	**13th International Conference on Electrostatics - Electrostatics 2011, Bangor University, Wales, UK:** Poster (P2.20), 'Electronic Memory Devices Based on an Organic Ferroelectric Polymer'
3.10. - 5.10.2010	**Polymers in Biomedicine and Electronics - Biannual Meeting of the GDCh-Division Macromolecular Chemistry, Berlin-Dahlem:** Poster (CharTra 11), 'Stability of Polarization in Organic Ferroelectric Metal-Insulator-Semiconductor Structures'

9.8. - 12.8.2010	**19th International Symposium on the Applications of Ferroelectrics, Edinburgh (UK):** Oral contribution (H8) 'Dielectric Investigation of an Organic Ferroelectric Insulator/Semiconductor Structure'
4.7. - 9.7.2010	**10th IEEE International Conference on Solid Dielectrics (ICSD), Potsdam:** Poster (C2-20), 'Influence of Lateral Currents on Capacitance Spectra of Organic Metal-Insulator-Semiconductor Structures with a Ferroelectric Insulator'
21.3. - 26.3.2010	**DPG Spring Meeting, Regensburg:** Oral Contribution (DF 10.9), 'Preparation and dielectric investigation of organic metal insulator semiconductor (MIS) structures with a ferroelectric polymer'
23.9. - 27.9.2009	**Joint Meeting of 12th International Meeting on Ferroelectricity (IMF-12), Xi'an (China):** Poster (FP-005) presented by P. Frübing, 'Preparation and Dielectric Investigation of Organic Metal-Insulator-Semiconductor (MIS) Structures with a Ferroelectric Polymer'

Publications

2011	R. Kalbitz, P. Frübing, R. Gerhard and D.M. Taylor, 'Organic electronic memory based on a ferroelectric polymer', Journal of Physics: Conference Series, Conference on Electrostatics, Reference Number: 3542 (pending)
2011	R. Kalbitz, P. Frübing, R. Gerhard and D.M. Taylor, 'Stability of Polarization in Organic Ferroelectric Metal-Insulator-Semiconductor Structures', Appl. Phys. Lett., 98,033303(3)

2010	R. Kalbitz, P. Frübing, R. Gerhard and D.M. Taylor, 'Influence of Lateral Currents on Capacitance Spectra of Organic Metal-Insulator-Semiconductor structures with a ferroelectric insulator', Proc. 10th IEEE ICSD, IEEE Catal. no. CFP10ICS-PRT, Digit. Ident.: 10.1109/ICSD.2010.5567939:410

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Statement of Authorship/ Selbstständigkeitserklärung

I hereby solemnly affirm that this thesis was written by myself and describes my own work, unless otherwise acknowledged in the text. The thesis has not been submitted for the award of any other degree in any other tertiary institution.

Hiermit erkläre ich, dass ich die vorliegend arbeit selbständig verfasst habe und keine anderen als die angegebenen Quellen und Hilfsmittel benutzt habe. Ferner erkläre ich, dass die Arbeit noch nicht in einem anderen Studiengang als Prüfungsleistung verwendet wurde.

Rene Kalbitz