A Methodology for Characterization, Modeling, and Mitigation of Single Event Transient Effects in CMOS Standard Combinational Cells

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ii

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Abstract

With the downscaling of CMOS technologies, the radiation-induced Single Event Transient (SET) effects in combinational logic have become a critical reliability issue for modern integrated circuits (ICs) intended for operation under harsh radiation conditions (e.g., in space). The SET pulses generated in combinational logic may propagate through the circuit and eventually be latched in storage elements (flip-flops or latches), resulting in soft errors and, consequently, in data corruption or system failure. It has thus become an imperative to address the SET effects in the early phases of the radiation-hard IC design. In general, the soft error mitigation solutions should accommodate both static and dynamic measures to ensure the optimal utilization of available resources. An efficient soft-error-aware design should address synergistically three main aspects: (i) characterization and modeling of soft errors, (ii) multi-level soft error mitigation, and (iii) online soft error monitoring. Although significant results have been achieved, the effectiveness of SET characterization methods, accuracy of predictive SET models, and efficiency of SET mitigation measures are still critical issues. Therefore, this work addresses the following topics:

- Characterization and modeling of SET effects in standard combinational cells,
- Static mitigation of SET effects in standard combinational cells, and
- Online particle detection, as a support for dynamic soft error mitigation.

Since the standard digital libraries are widely used in the design of radiation-hard ICs, the characterization of SET effects in standard cells and the availability of accurate SET models for the Soft Error Rate (SER) evaluation are the main prerequisites for efficient radiation-hard design. This work introduces an approach for the SPICE-based standard cell characterization with the reduced number of simulations, improved SET models and optimized SET sensitivity database. It has been shown that the inherent similarities in the SET response of logic cells for different input levels can be utilized to reduce the number of required simulations in the characterization process. Based on characterization results, the fitting models for the SET sensitivity metrics (critical charge, generated SET pulse width and propagated SET pulse width) have been developed. The proposed models are based on the principle of superposition, and they express explicitly the dependence of the SET sensitivity of individual combinational cells on design, operating and irradiation parameters. In contrast to the state-of-the-art characterization methodologies which employ extensive look-up tables (LUTs) for storing the raw simulation results, this work proposes the use of LUTs for storing the fitting coefficients of the SET sensitivity models derived from the characterization results. In that way the amount of characterization data in the SET sensitivity database is reduced significantly, which could potentially enable to speed up the subsequent SER evaluation of a given design.

The initial step in enhancing the robustness of combinational logic is the application of gate-level mitigation techniques. This is done selectively, i.e., the mitigation techniques are applied to the most sensitive gates (with the highest SER). As a result, significant improvement of the overall SER can be achieved with minimum area, delay and power overheads. For the SET mitigation in standard cells, it is essential to employ the techniques that do not require modifying the cell structure. This work introduces the use of decoupling cells for improving the robustness of standard combinational cells. By insertion of

two decoupling cells at the output of a target cell, the critical charge of the cell's output node is increased and the attenuation of short SETs is enhanced. In comparison to the most common gate-level techniques (gate upsizing and gate duplication), the proposed approach provides better SET filtering. However, as there is no single gate-level mitigation technique with optimal performance, a combination of multiple techniques is required. This work introduces a comprehensive characterization of gate-level mitigation techniques aimed to quantify their impact on the SET robustness improvement, as well as introduced area, delay and power overhead per gate. By characterizing the gate-level mitigation techniques together with the standard cells, the required effort in subsequent SER analysis of a target design can be reduced. The characterization database of the hardened standard cells can be utilized as a guideline for selection of the most appropriate mitigation solution for a given design.

As a support for dynamic soft error mitigation techniques that are applied at the system level, it is important to enable the online detection of energetic particles causing the soft errors. This allows activating the power-greedy fault-tolerant configurations based on N-modular redundancy (e.g., Triple Modular Redundancy) only at the high radiation levels. To enable such a functionality, it is necessary to monitor both the particle flux and the variation of particle LET, as these two parameters contribute significantly to the system SER. In this work, a particle detection approach based on custom-sized pulse stretching inverters is proposed. Employing the pulse stretching inverters connected in parallel enables to measure the particle flux in terms of the number of detected SETs, while the particle LET variations can be estimated from the distribution of SET pulse widths. This approach requires a purely digital processing logic, in contrast to the standard detectors for flux and LET monitoring (e.g., diode-based detectors) which require complex mixed-signal processing. Besides the possibility of LET monitoring, additional advantages of the proposed particle detector are low detection latency and power consumption, and immunity to error accumulation.

The results achieved in this thesis can serve as a basis for establishment of an overall soft-error-aware database for a given digital library, and a comprehensive multi-level radiation-hard design flow that can be implemented with the standard IC design tools. The following step will be to evaluate the achieved results with irradiation experiments.

Zusammenfassung

Mit der Verkleinerung der Strukturen moderner CMOS-Technologien sind strahlungsinduzierte Single Event Transient (SET)-Effekte in kombinatorischer Logik zu einem kritischen Zuverlässigkeitsproblem in integrierten Schaltkreisen (ICs) geworden, die für den Betrieb unter rauen Strahlungsbedingungen (z. B. im Weltraum) vorgesehen sind. Die in der Kombinationslogik erzeugten SET-Impulse können durch die Schaltungen propagieren und schließlich in Speicherelementen (z.B. Flip-Flops oder Latches) zwischengespeichert werden, was zu sogenannten *Soft-Errors* und folglich zu Datenbeschädigungen oder einem Systemausfall führt. Daher ist es in den frühen Phasen des strahlungsharten IC-Designs unerlässlich geworden, die SET-Effekte systematisch anzugehen. Im Allgemeinen sollten die Lösungen zur Minderung von Soft-Errors sowohl statische als auch dynamische Maßnahmen berücksichtigen, um die optimale Nutzung der verfügbaren Ressourcen sicherzustellen. Somit sollte ein effizientes Soft-Error-Aware-Design drei Hauptaspekte synergistisch berücksichtigen: (i) die Charakterisierung und Modellierung von Soft-Errors, (ii) eine mehrstufige-Soft-Error-Minderung und (iii) eine Online-Soft-Error-Überwachung. Obwohl signifikante Ergebnisse erzielt wurden, sind die Wirksamkeit der SET-Charakterisierung, die Genauigkeit von Vorhersagemodellen und die Effizienz der Minderungsmaßnahmen immer noch die kritischen Punkte. Deshalb befasst sich diese Arbeit mit den aktuellen Themen im Zusammenhang mit

- Charakterisierung und Modellierung von SET-Effekten in der Standardzellbibliothek
- Abschwächung von SET-Effekten in Standardzellen
- Online-Erkennung von Partikelflux- und LET-Variationen durch Messung der SETs

Da die digitalen Standardbibliotheken beim Entwurf von strahlungsharten ICs weit verbreitet sind, sind die Charakterisierung von SET-Effekten in Standardzellen und die Verfügbarkeit genauer SET-Modelle für die Bewertung der Soft Error Rate (SER) die Hauptvoraussetzungen für ein effizientes strahlungsharten Design. Diese Arbeit stellt einen Ansatz für die SPICE-basierte Standardzellcharakterisierung vor, der auf einer reduzierten Anzahl von Simulationen, verbesserten SET-Modellen und einer optimierten SET-Datenbank basiert. Es wurde gezeigt, dass die inhärenten Ähnlichkeiten in der SET-Antwort von Logikzellen unter verschiedenen Betriebseinstellungen verwendet werden können, um die Anzahl der erforderlichen Simulationen im Charakterisierungsprozess zu reduzieren. Basierend auf den Ergebnissen dieser Charakterisierung wurden Modelle für Metriken der SET-Empfindlichkeit wie kritische Ladung, erzeugte SET-Impulsbreite und propagierte SET-Impulsbreite erstellt. Diese Modelle drücken explizit den Einfluss der SETs auf die Entwurfs-, Betriebs- und Bestrahlungsparametern einer Schaltung aus. Solche Modelle können in Standardbibliotheken für verschiedene Technologien übernommen und als Grundlage für die SER-Bewertung eines Designs verwendet werden. Im Gegensatz zu den neuesten Charakterisierungs-methoden, bei denen umfangreiche Tabellen (Look-Up Tables, LUTs) zum Speichern der Simulations-ergebnisse verwendet werden, wird in dieser Arbeit die Speicherung der Anpassungskoeffizienten der SET-Sensitivitätsmodelle vorgeschlagen, die aus einer Charakterisierung entstehen. Auf diese Weise wird die Menge der Daten erheblich reduziert, wodurch die nachfolgende SER-Auswertung gegebenenfalls beschleunigt werden kann.

Der erste Schritt zur Verbesserung der Robustheit der kombinatorischen Logik ist die Anwendung von Techniken zur Minderung auf Gatter-Ebene. Dies erfolgt selektiv, d.h. die Techniken werden nur auf die empfindlichsten Gatter (mit dem höchsten SER) angewendet. Infolgedessen kann eine signifikante Verbesserung des gesamten SER mit minimalem Flächen-, Verzögerungs- und Leistungsaufwand erreicht werden. Für die SET-Minderung in Standardzellen ist es wichtig, die Techniken anzuwenden, die keine Modifikation der Zellstruktur erfordern. In dieser Arbeit wird die Verwendung von Entkopplungszellen zur Verbesserung der Robustheit von kombinatorischen Standardzellen vorgestellt. Durch Einfügen von zwei Entkopplungszellen am Ausgang eines Gatters wird die kritische Ladung des Ausgangsknotens dieser erhöht und eine Dämpfung kurzer SETs ermöglich. Im Vergleich zu den gängigen Techniken auf Gatter-Ebene (Upsizing und Duplizierung) bietet der vorgeschlagene Ansatz eine bessere SET-Filterung. Da es jedoch keine einzige Minderungstechnik auf Gatter-Ebene mit optimaler Leistung gibt, ist eine Kombination mehrerer Techniken erforderlich. In dieser Arbeit wird eine umfassende Charakterisierung von Techniken zur Minderung auf Gatter-Ebene vorgestellt, um deren Auswirkungen auf die Verbesserung der SET-Robustheit sowie den eingeführten Bereich, die Verzögerung und den Leistungsaufwand pro Gatter zu quantifizieren. Durch die Charakterisierung der Minderungstechniken auf Gatter-Ebene und den vorgeschlagenen robusteren Standardzellen kann der erforderliche Aufwand bei der anschließenden SER-Analyse eines Zieldesigns minimiert werden. Die Charakterisierungsdatenbank für die gehärteten Standardzellen auf Gatter-Ebene kann als Richtlinie für die Auswahl der am besten geeigneten Lösung für ein bestimmtes Design verwendet werden.

Zur Unterstützung dynamischer Techniken zur Minderung der Soft-Errors, ist es wesentlich eine Online-Überwachung energetischer Partikel auf Systemebene, zu ermöglichen. Dadurch können leistungshungrige, fehlertolerante auf N-modularer Redundanz basierende Konfigurationen (z. B. dreifache modulare Redundanz) nur unter den hohen Strahlungspegeln aktiviert werden. Um eine solche Funktionalität zu ermöglichen, ist es notwendig, sowohl den Partikelfluss als auch die Variation des Partikel-LET zu überwachen, da diese beiden Parameter wesentlich zum SER des Systems beitragen. In dieser Arbeit wird durch eigens dafür entwickelten Invertern, ein Ansatz zum Detektieren der Partikel vorgeschlagen. Die Verwendung dieser Zellen in einer parallelen Konfiguration ermöglicht die Messung des Partikelflusses in Bezug auf die Anzahl der erfassten SETs, während die Partikel-LET-Variation aus der Verteilung der verschiedenen SET-Impulsbreiten abgeschätzt werden kann. Dieser Ansatz erfordert eine einfache, rein digitale Verarbeitungslogik im Gegensatz zu den komplexeren Standarddetektoren für den Flux- und die LET-Überwachung (z. B. Detektoren auf Diodenbasis). Darüber hinaus sind die Möglichkeiten der LET-Überwachung, eine geringe Latenz, der geringe Stromverbrauch und die Immunität gegenüber einer Fehlerakkumulation die Hauptvorteile der hier vorgeschlagenen Lösung.

Die in dieser Arbeit erzielten Ergebnisse können als Grundlage für die Erstellung einer umfassenden Soft-Errors-Datenbank dienen, die zusammen mit einer Standardzellenbibliothek, eine vollständige mehrstufige strahlungsharte IC-Entwicklung unter der Verwendung gängiger IC-Entwurfswerkzeugen ermöglich. Der letzte Schritt besteht darin, die erzielten Ergebnisse durch Bestrahlungsexperimente zu bewerten.

Contents

Acknowledgement	v
Abstract	vii
Zusammenfassung	ix
List of Figures	xvi
List of Tables	xxi
List of Acronyms	xxiii
1. Introduction	
1.1 Motivation	
1.1.1 Soft Error Trends in CMOS Technologies	
1.1.2 Soft-Error-Aware Design Concept	5
1.1.3 SET Characterization and Modeling	6
1.1.4 Radiation Hardening Techniques	7
1.1.5 Online Soft Error Rate Monitoring	
1.2 Research Scope and Objectives	9
1.3 Thesis Contributions	
1.4 Thesis Organization	
1.5 Publications	
2. Basics of SET Effects	
2.1 Radiation Environments and Quantities	
2.2 SET Generation Mechanisms	
2.2.1 Charge Generation	
2.2.2 Charge Collection	
2.2.3 SET Current and Voltage Pulse Formation	
2.2.4 Charge Sharing and Single Event Multiple Transients	
2.3 SET Propagation Mechanisms	
2.3.1 SET Masking Effects	
2.3.2 Other SET Propagation Effects	
2.4 SET Sensitivity Metrics	

	2.4.1 C	ritical Charge (Q_{CRIT}) and LET Threshold (LET_{TH})	23
	2.4.2 S	ET Amplitude and Width	23
	2.4.3 S	oft Error Rate (SER)	24
	2.4.4 C	ross Section (σ)	25
2.5	5 Effect o	of CMOS Technology Scaling on SET Sensitivity	25
	2.5.1 C	ritical Charge (Threshold LET) Scaling	25
	2.5.2 S	ET Pulse Width Scaling	25
	2.5.3 C	ombinational SER Scaling	26
2.0	6 Parame	ters Affecting the SET Sensitivity	28
	2.6.1 Ir	npact of Technology Parameters	28
	2.6.2 Ir	npact of Design Parameters	29
	2.6.3 Ir	npact of Operating Parameters	30
	2.6.4 Ir	npact of Irradiation Parameters	31
	2.6.5 Ir	npact of Other Failure Mechanisms	32
	2.6.6 R	elative and Combined Impact of Multiple Parameters	32
3. R	elated V	Vork	33
3.	1 A Mult	ilevel Radiation-Hardening-By-Design Flow	33
3.2	2 SET Ch	aracterization in Combinational Logic	35
	3.2.1	Simulation-Based and Analytical Characterization Methodologies	35
	3.2.2	A Two-Phase Combinational SER Evaluation	37
	3.2.3	SET Characterization of Standard Cell Library	39
3.3	3 SET M	odels	43
	3.3.1	SET Current Models	44
	3.3.2	Critical Charge Models	48
	3.3.3	SET Pulse Width Models	
	3.3.4	SET Propagation Models	51
3.4	4 Gate-le	vel SET Mitigation Approaches	53
	3.4.1	Gate Upsizing	55
	3.4.2	Gate Duplication/Cloning	55
	3.4.3	Load Upsizing	56
	3.4.4	Guarded Dual Modular Redundancy	56
	3.4.5	Insertion of Charge Sharing Logic	57
	3.4.6	Insertion of Cross-Coupled Inverters	57
	3.4.7	Insertion of Schmitt Trigger	58
	3.4.8	Insertion of Transmission Gate	58

	3.4.9	Insertion of Guard Gate Filter	58
	3.4.10	Insertion of Cascaded Inverters	59
	3.4.11	Comparison of Gate-level Hardening Techniques	59
3.5	5 Particle	Detectors for On-line Soft Error Rate Monitoring	61
	3.5.1	Bulk Built-in Current Detectors	61
	3.5.2	Acoustic Wave Detectors	63
	3.5.3	Diode Detectors	63
	3.5.4	SRAM Detectors	64
	3.5.5	3D NAND Flash Detectors	65
	3.5.6	Comparison of Particle Detectors	65
3.6	5 Summa	ry of Open Issues Addressed in this Thesis	66
4. Cl	haracte	rization and Modeling of SET Effects in Standard Combinational Cells	68
		ction	
		tic Methodology for Standard Cell Library Characterization	
		neration Analysis	
		ritical Charge Analysis	
		ominal SER per Logic Gate	
		ET Pulse Width Analysis	
4.4		ppagation Analysis	
		ET Propagation through Single-Input Gates	
		ET Propagation through Multiple-Input Gates	
		verall Comparison of SET Propagation Effects	
		ET Propagation in Combinational Paths	
4.5		vare Design Considerations	
4.6	5 SET Se	nsitivity Models	101
	4.6.1 C	ritical Charge Model	101
	4.6.2 G	enerated SET Pulse Width Model	105
	4.6.3 P	ropagated SET Pulse Width Model	109
4.7	SET Ef	fects in Application-Specific Standard Cells	113
	4.7.1 S	ET and SEU Effects in a Muller-C Element	113
	4.7.2 S	ET Effects in a SEL Protection Switch	115
4.8	8 Optimiz	ation of SET Characterization Process	118
	4.8.1 R	eduction of Number of Simulations	119
	4.8.2 R	eduction of SET Database	121
4.9	Summa	ry	125

5. Mitigation of SET Effects in Standard Combinational Cells	
5.1 Introduction	
5.2 Concept of SET Mitigation with Decoupling Cells	
5.3 Analysis of SET Mitigation with Decoupling Cells	
5.3.1 Critical Charge Analysis	
5.3.2 Nominal SER Analysis	
5.3.3 SET Pulse Generation Analysis	
5.3.4 SET Pulse Propagation Analysis	
5.3.5 Application of Decoupling Cells to Combinational Paths	
5.4 Comparative Characterization of SET Mitigation Techniques	
5.4.1 Comparison of SET Sensitivity	
5.4.2 Comparison of Area, Delay and Power Overhead	
5.4.3 Comparison of SET Mitigation Efficiency	
5.5 Combined Application of Multiple SET Mitigation Techniques	
5.6 SET Mitigation in Standard Delay Cells	
5.7 Overall Comparison of SET Mitigation Techniques	
5.8 Summary	
6. Particle Detection with Pulse Stretching Inverters	
6.1 Introduction	
6.2 Design and Operation of a Pulse Stretching Cell (PSC)	
6.3 Characterization of Normal Operation of a PSC	
6.3.1 Impact of Technology	
6.3.2 Impact of Transistor Sizing	
6.3.3 Impact of Supply Voltage and Temperature	
6.3.4 Impact of the Number of Cascaded Pulse Stretchers	
6.4 Characterization of PSC as a Particle Detector	
6.4.1 SET Effects in a Single PSC	
6.4.2 SET Effects in PSCs Connected in Series	
6.4.3 SET Effects in PSCs Connected in Parallel	
6.4.4 Overall Comparison of Serial and Parallel PSC Configurations	
6.5 Readout Circuit Design	
6.5.1 Readout Circuit for Particle Flux Monitoring	
6.5.2 Readout Circuit for Particle Flux and LET Monitoring	
6.6 Comparison with the State-of-the-Art Particle Detectors	
6.7 Application in a Self-Adaptive Multi-Processor System	

6.8 Summary	
7. Conclusion	
7.1 Achieved Results	
7.2 Future Work	
Bibliography	

List of Figures

Figure 1. 1:	SoC scaling trends predicted by IRDS 2020 report [2]	1
Figure 1. 2:	Chip-level SER trends with technology scaling [38]	
Figure 1. 3:	Main elements of a soft-error-aware IC design concept	
Figure 2. 1:	Basic mechanisms of particle interaction with a p-n junction in CMOS	
-	inverter	17
Figure 2. 2:	Effect of particle strike in an inverter for low(0) and high(1) input levels	
Figure 2. 3:	Typical shape of SET current pulse for: (a) low LET and (b) high LET	19
Figure 2. 4:	Typical shapes of positive (0-to-1) SET pulse for different LET	
Figure 2. 5:	Effect of electrical, logical and temporal masking on SET propagation	
Figure 2. 6:	Measured SER (thick lines with symbols) and predicted SER (thin lines) as a	
	function of operating frequency, for sequential and combinational logic in 40	
	nm technology (reproduced from [44])	
Figure 3. 1:	A multilevel rad-hard design flow for standard-cell-based IC designs	
Figure 3. 2:	Hierarchy of multi-level simulation-based SET characterization	
Figure 3. 3:	A general two-phase combinational SER evaluation flow	
Figure 3. 4:	SET current models: micro-model (left) and macro-model (right)	
Figure 3. 5:	Bias-dependent current model proposed in [205, 206]	
Figure 3. 6:	Gate upsizing by replacing AND2_x1 with AND2_x2	
Figure 3. 7:	Duplication of AND gate: (a) standard variant, and (b) variant with clamping	
	diode	
Figure 3. 8:	SET mitigation by increasing the size of load gates	
Figure 3. 9:	GDMR implementation of AND gate	
Figure 3. 10:	SET mitigation in AND gate by with: (a) charge sharing logic, (b) cross-	
	coupled inverters	
Figure 3. 11:	SET mitigation with: (a) Schmitt trigger, and (b) transmission gates	
Figure 3. 12:	SET mitigation with (a) delay element and guard gate, (b) two cascaded	
	inverters	
Figure 3. 13:	BBICS implementation: (a) design of a PMOS-BBICS, and (b) connection of	
	two BBICSs to an inverter [263]	
Figure 3. 14:	A cross-section of cantilever structure for acoustic wave detection [270]	
Figure 3. 15:	Diode detectors with readout circuit	64
Figure 4. 1:	Proposed methodology for characterization and modeling of SET effects in	
	standard cells and corresponding hardened configurations	71
Figure 4. 2:	Simulation setup for characterization of SET effects in standard cells	73
Figure 4. 3:	Critical charge of inverter as a function of its size factor, for different load	
	sizes and both input levels, and for nominal supply voltage (1.2 V) and	
	temperature (27 °C)	76
Figure 4. 4:	Change of critical charge of INV gate as a function of the change of supply	
	voltage, for: (a) different driving strengths of target inverter, (b) different	
	driving strengths of load inverter	77

Figure 4. 5:	Change of critical charge of INV gate as a function of the change of temperature with respect to $T_{EMP} = 27$ °C, for different driving strengths of	
	INV gate and low input level	
Figure 4. 6:	Critical charge of INV gate as a function of rise and fall time constants of the	
	current pulse, for different driving strengths of INV gate and low input level	
Figure 4. 7:	Critical charge of two-input logic gates as a function of their driving strength	
	and input levels, while all other parameters are at nominal values	
Figure 4. 8:	SET pulse width for LET of 10, 30 and 60 MeVcm ² mg ⁻¹ : (a) SPICE	
	simulation results for INV_x1 gate, (b) minimum, average and maximum	
	values measured by Narasimhan et al. [115]	
Figure 4. 9:	SET pulse amplitude and width as a function of LET, for current injection in INV_x1	
Figure 4. 10:	SET pulse width as a function of LET: (a) for different driving strengths of	
	target inverter with low input level and INV_x1 as a load gate, and (b) for	
	INV_x1 as a target gate with low input level and different driving strengths	
	of load inverter	
Figure 4. 11:	SET pulse width for LET = 60 MeVcm ² mg ⁻¹ , as a function of: (a) driving	
	strengths of target inverter and load inverter, and (b) driving strength of target	
	inverter and number of INV_x1 load gates	
Figure 4. 12:		
	supply voltage, and (b) temperarure	
Figure 4. 13:	SET pulse width as a function of LET, for (a) NAND2_x1, and (b) NOR2_x1	
Figure 4. 14:	SET pulse width at the output of SDC_x1 and SDC_x2, when current pulse	
	is injected successively in each inverter within the cells, for low input level	
Figure 4. 15:	SET pulse width at the output of SDCs for supply voltage and temperature	
	corners	
Figure 4. 16:	SET pulse width at the output of standard combinational cells with x1 driving	
	strength, when the current pulse with $LET = 30 \text{ MeV cm}^2 \text{mg}^{-1}$ is injected in	
	most sensitive nodes	91
Figure 4. 17:	SET pulse width at the output of INV and BUF gates, as a function of their	
	driving strength, for: (a) positive input pulse of 200 ps, (b) negative input	
	pulse of 200 ps	
Figure 4. 18:	SET pulse width at the output of INV gate, as a function of its driving strength	
	and load capacitance, for: (a) positive input pulse of 200 ps, (b) negative input	
	pulse of 200 ps	
Figure 4. 19:	SET pulse width at the output of 2-, 3- and 4-input NAND and AND gates, as	
	a function of input SET pulse width	
Figure 4. 20:	SET pulse width in terms of LET, for inviter with minimum size factor as a	
T	target gate	
Figure 4. 21:	Comparison of generated SET pulse width from simulations and proposed	100
E 4.02	model, for INV, NAND2 and NOR2 gates	
	Van Berkel's C-element implementation and C-element truth table	114
Figure 4. 23:	Comparison of SET and SEU critical charge as a function of size factor of C-	114
	element, for INV_x1 as a load, and nominal supply voltage and temperature	

Figure 4. 24:	SPS cell block diagram	116
Figure 4. 25:	Critical charge of the output node of SPS cell as a function of W/L ratio of	
	PMOS sensing/driving transistor and number of load inverters N (for fixed	
	supply voltage, temperature and timing parameters of current pulse)	117
Figure 4. 26:	A generic example of four LUTs for storing the critical charge values in terms	
	of size factor of target gate, size factor of load gate and supply voltage, for	
	nominal values of all other parameters (for a single input vector, one sensitive	
	node and fixed timing parameters of current pulse)	
Figure 4. 27:	A generic 2D LUT for storing the coefficients for critical charge model, for a	
-	particular gate and all input vectors (for one sensitive node in target gate, and	
	fixed timing parameters of current pulse)	
Figure 4. 28:	A generic 2D LUT for storing the coefficients for generated SET pulse width	
	model, for a particular gate and all input vectors (for one sensitive node in	
	target gate, and fixed timing parameters of current pulse)	124
Figure 4. 29:	A generic 2D LUT for storing the coefficients for propagated SET pulse width	
0	model, for a particular gate and all input pins	124
Figure 5. 1:	Schematic of decoupling cell in CMOS technology; (a) with one NMOS	
-	transistor, (b) with cross-coupled NMOS and PMOS transistors	129
Figure 5. 2:	Application of two decoupling cells for improving the SET robustness of	
0	NAND gate	
Figure 5. 3:	Response of NAND2_x1 gate: (a) normal pulse after propagation through	
-	NAND2_x1 gate without and with decoupling cells, (b) SET pulses generated	
	at the output of NAND2_x1 gate without and with decoupling cells	131
Figure 5. 4:	Absolute and normalized Q _{CRIT} when two decoupling cells with driving	
0	strengths x1, x2 and x4 are inserted successively at the output of 1-input gates	
	(for all input levels)	
Figure 5. 5:	Absolute and normalized Q _{CRIT} when two decoupling cells with driving	
0	strengths x1, x2 and x4 are inserted successively at the output of 2-input gates	
	(for all input levels)	
Figure 5. 6:	Absolute and normalized Q _{CRIT} when two decoupling cells with driving	
0	strengths x1, x2 and x4 are inserted successively at the output of 2-, 3- and 4-	
	input NAND gate (for low input levels)	134
Figure 5. 7:	Absolute and normalized SER for 1- and 2-input standard logic gates with	
0	and without decoupling cells with size factor x1, for most sensitive input	
	levels	137
Figure 5. 8:	SET pulse width at the output of NAND2_x1 gate as a function of LET, when	
C	decoupling cells with driving strengths x1, x2 and x4 are applied successively	
	(for all input levels)	
Figure 5. 9:	Effect of decoupling cells on SET filtering for NAND2 and NOR2 gates	
Figure 5. 10:	Homogeneous path with NAND gates and decoupling cells at nodes 4 and 8	
Figure 5. 11:		
0	nodes 3 and 7	
Figure 5. 12:	SET pulse width at the output of a 10-gate NAND chain as a function of LET,	
C I	for different positions of decoupling cells with size factor x4	143

Figure 5. 13:	SET pulse width at the output of a 10-gate NAND-NOR chain as a function	
	of LET, for different positions of decoupling cells with size factor x4	143
Figure 5. 14:	Normalized critical charge for standard (non-hardened) NAND2_x1 gate and	
	NAND2_x1 gate with hardening configurations (for 11 input)	147
Figure 5. 15:	Dependence of critical charge on size factor of applied hardening configu-	
	ration (for NAND2_x1 gate with 11 input)	147
Figure 5. 16:	Generated SET pulse width at the output NAND2_x1 gate without and with	
	hardening configurations with size factor x1, for $LET = 5 \text{ MeV}\text{cm}^2\text{mg}^{-1}$	149
Figure 5. 17:	Output SET pulse width as a function of input SET pulse width, for	
	NAND2_x1 gate and hardening configurations with size factor x4	151
Figure 5. 18:	Output SET pulse width as a function of input SET pulse width, for NOR2_x1	
	gate and hardening configurations with size factor x4	151
Figure 5. 19:	SET mitigation efficiency of analyzed hardening techniques considering the	
	relation between critical charge and area overhead, for size factor x1 of	
	hardening configurations (higher SME value is better)	155
Figure 5. 20:	SET pulse width at the output of a 10-gate NAND-NOR path as a function of	
	LET, for standard (non-hardened) path and for path with various combi-	
	nations of mitigation techniques: (a) for LET from 0.5 to 30 MeVcm ² mg ⁻¹ ,	
	and (b) for LET from 0.5 to 5 MeVcm ² mg ⁻¹	156
Figure 5. 21:	SET mitigation in standard delay cells with complete duplication	158
Figure 5. 22:	SET mitigation in standard delay cells with partial duplication	
Figure 6. 1:	A two-inverter pulse stretching cell (PSC)	164
Figure 6. 2:	Proposed symbol of two-inverter pulse stretching cell (PSC)	165
Figure 6. 3:	Simulation setup for analysis of normal operation of PSC	166
Figure 6. 4:	Stretching of 100 ps pulse with a single PSC in 130 nm and 250 nm techno-	
	logies	167
Figure 6. 5:	Output pulse width as a function of: (a) size factor S, (b) transistor size (for S	
	= 5)	168
Figure 6. 6:	Output pulse width as a function of: (a) normalized supply voltage, (b)	
	temperature	169
Figure 6. 7:	Output pulse width as a function of the number of cascaded pulse stretchers	169
Figure 6. 8:	SET response of PSC due to a particle strike in off-state NMOS transistor	170
Figure 6. 9:	Simulation setup for analysis of SET response of PSC	172
Figure 6. 10:	Dependence of LET _{TH} on channel length of on-state transistors (PMOS1 and	
-	NMOS2)	173
Figure 6. 11:	Dependence of LET _{TH} on channel width of off-state transistors (NMOS1 and	
-	PMOS2)	173
Figure 6. 12:	Output pulse width of a single PSC as a function of LET	174
Figure 6. 13:	LET _{TH} for two inverters in a single PSC as a function of supply voltage	175
Figure 6. 14:	LET _{TH} for two inverters in a single PSC as a function of temperature	175
-	Serial PSC configuration	
e	LET _{TH} and corresponding output SET pulse width when current pulse is	
-	successively injected in each inverter in a chain composed of 20 pulse	
	stretching inverters (10 PSCs)	177

Figure 6. 17:	Output SET pulse width as a function of LET, when the current pulse is	
	injected in the first and last inverters of a chain composed of 20 pulse	
	stretching inverters (10 PSCs)	177
Figure 6. 18:	SET response due to simultaneous current injection in two inverters of a 20-	
	inverter pulse stretching chain	178
Figure 6. 19:	SET pulse width at the output of a 20-inverter pulse stretching chain, as a	
	function of supply voltage, for $LET = 10 \text{ MeV cm}^2 \text{mg}^{-1}$ and temperature of 27	
	°C	178
Figure 6. 20:	Change of SET pulse width at the output of a 20-inverter pulse stretching	
	chain, as a function of temperature, for LET = $10 \text{ MeV cm}^2 \text{mg}^{-1}$ and supply	
	voltage of 1.2 V	179
Figure 6. 21:	Parallel PSC configuration	
Figure 6. 22:	Threshold LET of Inverter 1 and Inverter 2 in a PSC, for different number of	
	PSCs connected in parallel	
Figure 6. 23:	SET pulse width as a function of LET and number of cells connected in	
	parallel, when the current pulse is injected in second inverter in PSC	
Figure 6. 24:	SET pulse width as a function of LET and number of cells connected in	
	parallel, when the current pulse is injected in second inverter in PSC	
Figure 6. 25:	Change of SET pulse width at the output of one PSC in a 12-cell parallel	
	array, as a function of supply voltage and temperature, for LET = 10	
	MeVcm ² mg ⁻¹	
Figure 6. 26:	Change of SET pulse width at the output of one PSC in a 12-cell parallel	
	array, as a function of supply voltage and temperature, for LET = 10	
	MeVcm ² mg ⁻¹	
Figure 6. 27:	Particle detector based on a long PSC chain	
Figure 6. 28:	Readout circuit for particle detector based on a long PSC chain	
Figure 6. 29:	Particle detector based on multiple short PSC chains	
Figure 6. 30:	Readout circuit for particle detector based on multiple short PSC chains	
e	Particle detector based on PSCs connected in parallel	
Figure 6. 32:	Readout circuit for particle detector based on PSCs connected in parallel	
Figure 6. 33:	A self-adaptive microprocessor platform with online SER monitoring	194

List of Tables

Table 2. 1:	Measured SET pulse widths for bulk CMOS technologies	
Table 3. 1:	Summary of methodologies for SET characterization of standard cell libraries	41
Table 3. 2:	Comparison of SET current models	47
Table 3. 3:	Comparison of gate-level SET mitigation techniques	60
Table 3. 4:	Comparison of soft error (particle) detectors	
Table 4. 1:	Parameters analyzed in simulations	73
Table 4. 2:	Critical charge for INV gate with driving strengths x1, x2 and x4, for various load	
	configurations and low input level	77
Table 4. 3:	Q _{CRIT} for output node of NAND3	
Table 4. 4:	Q _{CRIT} for output node of AND3	
Table 4. 5:	Q _{CRIT} for output node of NAND4	
Table 4. 6:	Q _{CRIT} for output node of AND4	
Table 4. 7:	Nominal SER for INV_x1, for corner cases for supply voltage and temperature	
Table 4. 8:	Nominal SER for logic gates with driving strengths x1 and x2 ($V_{DD} = 1.2 \text{ V}$, $T_{EMP} = 27 ^{\circ}\text{C}$)	83
Table 4. 9:	Channel width (W) and length (L) for transistors in SDCs	
	SET pulse widths at the outputs of standard logic cells with driving streight x1,	
1 auto 4. 10.	when the current is injected in the output node	01
Table 4 11.	SET pulse width at the output of INV_x1 in terms of supply voltage, for positive	
1 4010 4. 11.	input pulses	95
Table 4 12.	SET pulse width at the output of BUF_x1 in terms of supply voltage, for positive	
10010 4. 12.	input pulses	95
Table 4 13.	SET pulse width at the outputs of INV and BUF gates, in terms of temperature, for	
1000 4.15.	$V_{DD} = 1.2$ V and positive input pulse of 200 ps	95
Table 4 14.	SET pulse width at the outputs of NAND and AND gates, in terms of supply vol-	
1 4010 4. 14.	tage, for positive input pulse of 200 ps	96
Table 4 15.	SET pulse width at the outputs of NAND and AND gates, in terms of temperature,	
1000 4.15.	for positive input pulse of 200 ps	97
Table 4 16.	SET pulse widths at the outputs of logic gates, for positive and negative input	
1000 4.10.	pulses of 50, 100 and 200 ps (for driving strength x_1 , INV_ x_1 as a load gate, V_{DD}	
	= 1.2 V and T_{EMP} = 27 °C)	
Table 4 17.	SET pulse widths at the outputs of combinational paths, for positive and negative	
1 4010 4. 17.	input pulses of 200 ps, for Low-VT ($V_{DD} = 1.08$ V, $T_{EMP} = -40$ °C), Typical-VT	
	$(V_{DD} = 1.2 \text{ V}, T_{EMP} = 25 \text{ °C})$ and High-VT $(V_{DD} = 1.32 \text{ V}, T_{EMP} = 125 \text{ °C})$	90
Table 4 18.	Comparison of critical charge obtained with proposed model and SPICE simula-	
1000 4. 10.	tions, for different setting for INV, NAND2 and NOR2 gates	104
Table 4 19.	Description of combinational paths used for model verification	
	Comparison of SET propagation through combinational paths from Table 4.19,	
1 4010 7, 20,	with proposed model and SPICE simulations, when the current pulse with LET =	
	$10 \text{ MeV cm}^2\text{mg}^{-1}$ is injected in the output node of first gate in each path	112
	To the vent mg is injected in the output node of mst gate in each path	

	Comparison of critical charge obtained with proposed model and SPICE simula-	
	tions for C-element designed in 130 and 65 nm technologies	115
	Comparison of critical charge obtained with proposed model and SPICE simula-	
	tions for SEL protection switch designed in 130 and 250 nm technologies	118
Table 4. 23:	Number of simulation runs for characterization of SET generation sensitivity of	
	standard logic cells, for standard and optimized characterization approaches	121
Table 4. 24:	Number of LUTs and elements in LUTs for storing the critical charge values for	
	one gate type, obtained from standard characterization	123
Table 4. 25:	Number of LUTs and elements in LUTs for storing the model coefficients for one	
	gate type	
	Transistor size and area for decoupling cells in 130 nm technology	132
Table 5. 2:	Critical charge for standard logic gates without and with applied decoupling cells,	
	when the current pulse is injected successively in the output node of target gate	
	and in decoupling cells connected to the gate (for the most sensitive input levels)	136
Table 5. 3:	Width of SET pulse generated at the output of logic gates with driving strength x1,	
	when the current pulse with $LET = 1 \text{ MeV cm}^2 \text{mg}^{-1}$ is injected in the output of each	
	gate (for the most sensitive input levels)	139
Table 5. 4:	Minimum pulse width that can propagate through a logic gate with drive strength	
	x1, without and with decoupling cells	
	Gate-level hardening configurations analyzed in this work	144
Table 5. 6:	Critical charge at the output node of a target gate (for the most sensitive input	
	levels)	146
	Generated SET pulse width for standard logic gates without hardening and with	
	hardening configurations with size factor x1, for $LET = 1 \text{ MeV}\text{cm}^2\text{mg}^{-1}$	148
	Propagated SET pulse width for standard logic gates without hardening and with	
	hardening configurations with size factor x1, for positive input pulse of 100 ps	150
Table 5. 9:	Normalized area for standard logic gates without and with hardening configura-	
	tions with size factor x1	152
Table 5. 10:	Propagation delay of a chain composed of driving buffer, target gate and load inv-	
	erter, without and with hardening configurations with size factor x1	153
Table 5. 11:	Normalized power overhead for standard logic gates without hardening and with	
	applied hardening configurations with size factor x1	153
Table 5. 12:	SET pulse width at the output of NAND-NOR path for $LET = 30 \text{ MeV cm}^2\text{mg}^{-1}$,	
	propagation delay of the path without and with mitigation configurations, and	
	corresponding SET mitigation efficiency SME (SET pulse width, delay)	157
	SET pulse width at the output of standard delay cells, for standard version and two	
	hardened configurations (for low input level and LET = 30 MeVcm ² mg ⁻¹)	159
Table 5. 14:	Normalized area and propagation delay for standard delay cells (SDC) with driving	
	strength x1 and x2, and corresponding hardened configurations (SDC_CD and	
	SDC_PD)	
	LET _{TH} for standard logic cells and SRAM cell in IHP's 130 nm technology	
Table 6. 2:	Transistor sizes for parallel PSC configuration	
Table 6. 3:	SET pulse width ranges for a PSC in a 12-cell array	
Table 6. 4:	SET pulse width ranges for standard cells in 130 nm library	
Table 6. 5:	Comparison of proposed particle detector with existing solutions	192

List of Acronyms

ASETAnalog Single Event TransientASICApplication Specific Integrated CircuitBBICSBulk Built-in Current SensorCECumulative EffectsCMOSComplementary Metal Oxide SemiconductorCPUCentral Processing UnitCSLCharge Sharing LogicDDDisplacement DamageDECAPDecoupling cellDMRDigital Single Event TransientDVFSDynamic Voltage and Frequency ScalingECLEnror Detection and CorrectionELTEnclosed Layout TransistorESSCEuropean Space AgencyFSMFinFeld Effect TransistorFITFin Field Effect TransistorFITGate DuplicationGDMRGate DuplicationGDMRGate UplicationGDMRGate UplicationGDMRGate UplicationGUInternational Roadmap for Devices and SystemsItDLInterational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad UpiszingLULoakup Table	ALPEN	Alpha Particle Source Drain Penetration
BBICSBulk Built-in Current SensorCECumulative EffectsCMOSComplementary Metal Oxide SemiconductorCPUCentral Processing UnitCSLCharge Sharing LogicDDDisplacement DamageDECAPDecoupling cellDMRDual Modular RedundancyDSETDigital Single Event TransientDVFSDynamic Voltage and Frequency ScalingECLEmitter Coupled LogicEDACEuropean Space AgencyESAEuropean Space AgencyESDElectrostatic DischargeFinFETFin Field Effect TransistorFTTGate DuplicationGDMRGuarded Dual Modular RedundancyGDUGate DuplicationFITFiallures in TimeGDGate UpsizingHILHardware Description LanguageICInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	ASET	Analog Single Event Transient
CECumulative EffectsCMOSComplementary Metal Oxide SemiconductorCPUCentral Processing UnitCSLCharge Sharing LogicDDDisplacement DamageDECAPDecoupling cellDMRDual Modular RedundancyDSETDigital Single Event TransientDVFSDynamic Voltage and Frequency ScalingECLError Detection and CorrectionEDACError Detection and CorrectionESAEuropean Space AgencyESQElectrostatic DischargeFinFETFin Field Effect TransistorFITGate OpplicationGDMRGated Dual Modular RedundancyGPUGatel OpplicationGLGate UppizingHDLHardware Description LanguageICInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	ASIC	Application Specific Integrated Circuit
CMOSComplementary Metal Oxide SemiconductorCPUCentral Processing UnitCSLCharge Sharing LogicDDDisplacement DamageDECAPDecoupling cellDMRDual Modular RedundancyDSETDigital Single Event TransientDVFSDynamic Voltage and Frequency ScalingECLEmitter Coupled LogicEDACError Detection and CorrectionELTEnclosed Layout TransistorESAEuropean Space AgencyESCCEuropean Space Components CoordinationESDElectrostatic DischargeFinFETFin Field Effect TransistorFITGate DuplicationGDGate UpilcationGDUGraphics Processing UnitGUGate UpsizingHDLHardware Description LanguageICInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	BBICS	Bulk Built-in Current Sensor
CPUCentral Processing UnitCSLCharge Sharing LogicDDDisplacement DamageDECAPDecoupling cellDMRDual Modular RedundancyDSETDigital Single Event TransientDVFSDynamic Voltage and Frequency ScalingECLEmitter Coupled LogicEDACError Detection and CorrectionELTEuropean Space AgencyESCEuropean Space Components CoordinationESDElectrostatic DischargeFinFETFin Field Effect TransistorFITGate DuplicationGDGate DuplicationGDUGraphics Processing UnitGUGate UpsizingHDLIntegrated CircuitIRDSInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	CE	Cumulative Effects
CSLCharge Sharing LogicDDDisplacement DamageDECAPDecoupling cellDMRDual Modular RedundancyDSETDigital Single Event TransientDVFSDynamic Voltage and Frequency ScalingECLEmitter Coupled LogicEDACError Detection and CorrectionELTEnclosed Layout TransistorESAEuropean Space AgencyESDElectrostatic DischargeFinFETFin Field Effect TransistorFITSaitures in TimeGDGate DuplicationGDUGraphics Processing UnitGUGate UpsizingHDLIntegrated CircuitIRDSInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	CMOS	Complementary Metal Oxide Semiconductor
DDDisplacement DamageDECAPDecoupling cellDMRDual Modular RedundancyDSETDigital Single Event TransientDVFSDynamic Voltage and Frequency ScalingECLEmitter Coupled LogicEDACError Detection and CorrectionELTEnclosed Layout TransistorESAEuropean Space AgencyESCCEuropean Space Components CoordinationESDElectrostatic DischargeFinFETFailures in TimeGDGate DuplicationGDWRGuarded Dual Modular RedundancyGPUGate UpsizingHDLHardware Description LanguageICInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	CPU	Central Processing Unit
DECAPDecoupling cellDMRDual Modular RedundancyDSETDigital Single Event TransientDVFSDynamic Voltage and Frequency ScalingECLEmitter Coupled LogicEDACEmitter Coupled LogicEDACEnclosed Layout TransistorELTEnclosed Layout TransistorESAEuropean Space AgencyESDElectrostatic DischargeFinFETFailures in TimeGDGate DuplicationGDMRGated Dual Modular RedundancyGPUGraphics Processing UnitGUGate UpsizingHDLHardware Description LanguageICInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULinear Energy Transfer	CSL	Charge Sharing Logic
DMRDual Modular RedundancyDSETDigital Single Event TransientDVFSDynamic Voltage and Frequency ScalingECLEmitter Coupled LogicEDACError Detection and CorrectionELTEnclosed Layout TransistorESAEuropean Space AgencyESDElectrostatic DischargeFinFETFin Field Effect TransistorFITFailures in TimeGDGate DuplicationGDWRGated Dual Modular RedundancyGPUGraphics Processing UnitGUIntegrated CircuitIRDSIntegrated CircuitIRDSInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	DD	Displacement Damage
DSETDigital Single Event TransientDVFSDynamic Voltage and Frequency ScalingECLEmitter Coupled LogicEDACError Detection and CorrectionELTEnclosed Layout TransistorESAEuropean Space AgencyESDElectrostatic DischargeFinFETFin Field Effect TransistorGDGate DuplicationGDGate DuplicationGDUGate dupsizingHDLIntegrated CircuitIRDSIntegrated CircuitLETLinear Energy TransferLULoad Upsizing	DECAP	Decoupling cell
DVFSDynamic Voltage and Frequency ScalingECLEmitter Coupled LogicEDACError Detection and CorrectionELTEnclosed Layout TransistorESAEuropean Space AgencyESCCEuropean Space Components CoordinationESDElectrostatic DischargeFinFETFin Field Effect TransistorFITGate DuplicationGDGate DuplicationGPUGraphics Processing UnitGUGate UpsizingHDLInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	DMR	Dual Modular Redundancy
ECLEmitter Coupled LogicEDACError Detection and CorrectionELTEnclosed Layout TransistorESAEuropean Space AgencyESCCEuropean Space Components CoordinationESDElectrostatic DischargeFinFETFin Field Effect TransistorFITFailures in TimeGDGate DuplicationGPUGraphics Processing UnitGUGate UpsizingHDLHardware Description LanguageICInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	DSET	Digital Single Event Transient
EDACError Detection and CorrectionELTEnclosed Layout TransistorESAEuropean Space AgencyESCCEuropean Space Components CoordinationESDElectrostatic DischargeFinFETFin Field Effect TransistorFITFailures in TimeGDGate DuplicationGPUGraphics Processing UnitGUGate UpsizingHDLHardware Description LanguageICIntegrated CircuitIRDSInternational Roadmap for Devices and SystemsLETLoad Upsizing	DVFS	Dynamic Voltage and Frequency Scaling
ELTEnclosed Layout TransistorESAEuropean Space AgencyESCCEuropean Space Components CoordinationESDElectrostatic DischargeFinFETFin Field Effect TransistorFITFailures in TimeGDGate DuplicationGPUGated Dual Modular RedundancyGUGate UpsizingHDLHardware Description LanguageICIntegrated CircuitIRDSInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	ECL	Emitter Coupled Logic
ESAEuropean Space AgencyESCCEuropean Space Components CoordinationESDElectrostatic DischargeFinFETFin Field Effect TransistorFITFailures in TimeGDGate DuplicationGDMRGuarded Dual Modular RedundancyGPUGraphics Processing UnitGUGate UpsizingHDLHardware Description LanguageICIntegrated CircuitIRDSInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	EDAC	Error Detection and Correction
ESCCEuropean Space Components CoordinationESDElectrostatic DischargeFinFETFin Field Effect TransistorFITFailures in TimeGDGate DuplicationGDMRGuarded Dual Modular RedundancyGPUGraphics Processing UnitGUGate UpsizingHDLHardware Description LanguageICIntegrated CircuitIRDSInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	ELT	Enclosed Layout Transistor
Fin Fin Fin Fin Fin Fin Field Effect DischargeFin FETFin Field Effect TransistorFITFailures in TimeGDGate DuplicationGDMRGuarded Dual Modular RedundancyGPUGraphics Processing UnitGUGate UpsizingHDLHardware Description LanguageICIntegrated CircuitIRDSInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	ESA	European Space Agency
FinFETFin Field Effect TransistorFITFailures in TimeGDGate DuplicationGDMRGuarded Dual Modular RedundancyGPUGraphics Processing UnitGUGate UpsizingHDLHardware Description LanguageICIntegrated CircuitIRDSInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	ESCC	European Space Components Coordination
FITFailures in TimeGDGate DuplicationGDMRGuarded Dual Modular RedundancyGPUGraphics Processing UnitGUGate UpsizingHDLHardware Description LanguageICIntegrated CircuitIRDSInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	ESD	Electrostatic Discharge
GDGate DuplicationGDMRGuarded Dual Modular RedundancyGPUGraphics Processing UnitGUGate UpsizingHDLHardware Description LanguageICIntegrated CircuitIRDSInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	FinFET	Fin Field Effect Transistor
GDMRGuarded Dual Modular RedundancyGPUGraphics Processing UnitGUGate UpsizingHDLHardware Description LanguageICIntegrated CircuitIRDSInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	FIT	Failures in Time
GPUGraphics Processing UnitGUGate UpsizingHDLHardware Description LanguageICIntegrated CircuitIRDSInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	GD	Gate Duplication
GUGate UpsizingHDLHardware Description LanguageICIntegrated CircuitIRDSInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	GDMR	Guarded Dual Modular Redundancy
HDLHardware Description LanguageICIntegrated CircuitIRDSInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	GPU	Graphics Processing Unit
ICIntegrated CircuitIRDSInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	GU	Gate Upsizing
IRDSInternational Roadmap for Devices and SystemsLETLinear Energy TransferLULoad Upsizing	HDL	Hardware Description Language
LETLinear Energy TransferLULoad Upsizing	IC	Integrated Circuit
LU Load Upsizing	IRDS	International Roadmap for Devices and Systems
	LET	Linear Energy Transfer
LUT Look-up Table	LU	Load Upsizing
	LUT	Look-up Table

Multiple Node Charge Collection
Process Design Kit
Propagation-induced Pulse Broadening
Pulse Stretching Cell
Quadruple Modular Redundancy
Radiation Hardening by Design
Radiation Hardening by Process
Radiation Hardening by Shielding
Register Transfer Level
Single Event Effect
Single Event Latchup
Single Event Multiple Transients
Soft Error Rate
Single Event Transient
Single Event Upset
System on Chip
Silicon on Insulator
Solar Particle Event
Simulation Program with Integrated Circuit Emphasis
Single Event Latchup Protection Switch
Schmitt Trigger
Technology Computer Aided Design
Transmission Gate
Total Ionizing Dose
Triple Modular Redundancy
Transistor-Transistor Logic

Chapter 1

Introduction

1.1 Motivation

The Complementary Metal-Oxide Semiconductor (CMOS) technologies are nowadays dominantly used for implementing the Application Specific Integrated Circuits (ASICs). In comparison with alternative technologies, such as Emitter Coupled Logic (ECL) and Transistor-Transistor Logic (TTL), the major advantages of CMOS technologies are lower power consumption and cost of implementation. Since the invention of first CMOS circuit by Wanlass and Sah in 1963 [1], the CMOS technologies have undergone continuous evolution through the reduction of transistor feature size and supply voltage. As a result, over the past 50 years the feature size has decreased from 10 μ m to 5 nm, and the supply voltage from 5 V to less than 1 V. This has brought the benefits in terms of increased transistor count per chip, reduced power consumption per transistor and higher clock frequencies, enabling to integrate more functions in a single System-on-Chip (SoC). According to the projections of the International Roadmap for Devices and Systems (IRDS) for the period 2020 – 2034, the forthcoming CMOS technologies are expected to maintain the clock frequency of SoCs in the range 2.8 – 3.6 GHz, with the decrease of supply voltage to 0.6 V, and exponential increase of the number of logic and memory cells, central processing units (CPU cores) and graphics processing units (GPU cores) in a single SoC, as illustrated in Figure 1.1 [2].

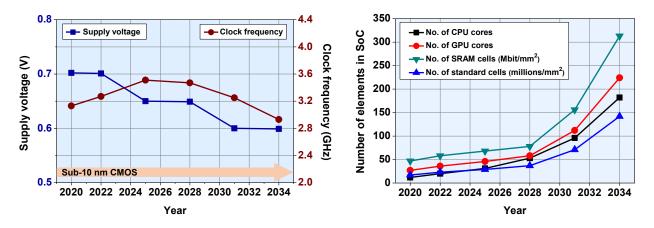


Figure 1. 1: SoC scaling trends predicted by IRDS 2020 report [2]

With the advancement of semiconductor technologies and the increasing complexity of nanoscale integrated circuits (ICs), the capabilities of electronic systems for the real-time data processing are continuously improving. This has led to the adoption of a broad spectrum of disruptive technologies in all segments of our everyday life, from general purpose consumer electronics to safety- and mission-critical applications (e.g., medicine, electric power plants, banking, automotive, aviation, space, etc.). However, the shrinking of transistor size, increase of transistor count per chip and aggressive scaling of supply voltage have resulted in new reliability threats in modern CMOS technologies, rendering the nanoscale ICs more and more prone to a wide variety of faults that can eventually result in temporary or permanent system failure. The faulty response of an IC may be caused either by physical mechanisms inherent in semiconductor technology or by environmental conditions. Therefore, it has become mandatory for IC designers to consider the reliability as a major design metric besides the standard metrics related to area, power consumption and performance. Some of the most common sources of failures in nanoscale ICs include manufacturing defects, process variations, aging, electrostatic discharge, crosstalk-induced noise, electric and electromagnetic interference, and radiation-induced effects.

Among the aforementioned reliability threats, the ionizing radiation effects are a major reliability issue for electronics employed in aerospace domain (satellites, spacecraft, and airplanes), as well as in terrestrial applications such as high-energy physics research and nuclear power stations. Moreover, as a result of technology downscaling, the ionizing radiation effects have become a growing reliability concern even for safety-critical terrestrial applications such as servers [3], automotive electronics [4, 5] and biomedical devices [6, 7]. Therefore, the radiation hardness has emerged as a key requirement in the design of fault-tolerant ICs. Along with that, the demand for radiation-hardened (rad-hard) electronics exhibits continuous growth. According to the market analysis report [8], the value of global rad-hard market was estimated to 1.45 billion USD in 2018, with the projected rise to approximately 1.7 billion USD in 2023. The increased demand for rad-hard electronics largely stems from the fact that many terrestrial applications rely on the support of communication satellites by more than 50 % over the past few years, resulting in 2787 operational satellites in 2020 [9]. The emerging concepts such as the Internet-of-Space, space solar energy farms and space tourism are likely to increase further the demand for rad-hard electronics.

Generally, the radiation-induced effects in electronic circuits can be divided in two groups: Cumulative Effects (CEs) and Single Event Effects (SEEs). The CEs are related to the long-term degradation of device's electrical characteristics by ionizing radiation, resulting from either the Total Ionizing Dose (TID) [10, 11] or the Displacement Damage (DD) [12, 13]. On the other side, SEEs represent the electrical disturbance in the circuit caused by the passage of a single energetic particle through a sensitive transistor, and can be classified as: soft (non-destructive) SEEs and hard (destructive) SEEs. The soft SEEs can result in temporary errors known as soft errors, but do not cause physical damage to the hardware. On the other hand, the hard SEEs can cause physical damage and permanent failure of a device, circuit or system. A detailed description of different types of SEEs can be found in [14 - 16]. Whereas the modern CMOS technologies are highly robust against the CEs and hard SEEs, the sensitivity to soft errors increases dramatically with technology downscaling. The soft errors denote the unwanted change of the logic state of sequential or memory elements (flip-flops, latches and SRAM cells). Although these errors disappear with resetting, power cycling or data overwrite [16], they can result in data corruption and temporary system failure. Apart

from the energetic particles, the soft errors can be also induced by the electromagnetic and electric noise, but these scenarios are less critical for modern ICs.

The radiation-induced soft errors in space (in registers in an orbital satellite) were first reported by Binder *et al.* in 1975 [17]. In 1976, the first case of soft errors at terrestrial level (in a laboratory computer) was recorded [18]. Since then, numerous evidences of soft errors in space and terrestrial applications have been published [3 - 7, 19 - 26]. In principle, a soft error can be caused by two types of SEEs:

- *Single Event Transient (SET)* a voltage pulse (glitch) induced at the output of a logic cell (gate) when an energetic particle hits a sensitive transistor in the cell and deposits a certain amount of charge beyond the threshold level (SET critical charge). To cause a soft error, an SET pulse must propagate through the subsequent logic gates and be latched by a memory or sequential element.
- *Single Event Upset (SEU)* a change of a logic value (bit flip) in a memory/sequential cell when an energetic particle hits a sensitive transistor in the cell and deposits a certain amount of charge beyond the threshold level (SEU critical charge).

Despite their temporary nature, the soft errors induce higher failure rate than all other unreliability mechanisms together [27]. Therefore, the design of radiation-hardened electronic systems requires comprehensive methodologies and models for predictive analysis of the soft error effects and efficient hardening measures to mitigate these effects. Traditionally, the SEUs have been the major contributor to soft errors and are often regarded as a synonym for soft errors, while the SETs have been usually neglected because of their weaker impact. However, **as CMOS technologies continue to scale down and new design paradigms are adopted, the contribution of SETs to the soft errors increases significantly**, turning SETs into a reliability risk that must be thoroughly addressed in all phases of the rad-hard IC design.

This work aims to advance the state-of-the-art by enhancing the SET characterization, modeling and mitigation methods. The common IC design approach is based on the use of standard cell libraries which are not designed to be rad-hard, and the conventional IC design tools are not optimized for analysis of radiation-induced effects. Besides, due to the increased complexity of modern ICs as well as the variable radiation environments (e.g. space), there is a need for both static and dynamic soft error mitigation solutions in order to achieve a trade-off between performance, reliability and power consumption. In that regard, this work particularly addresses the following topics:

- Characterization and modeling of SET effects in standard combinational cells,
- Static mitigation of SET effects in standard combinational cells, and
- Online particle detection, as a support for dynamic soft error mitigation.

The following discussion further elaborates the need for addressing the SET effects in the rad-hard design, with a brief overview of limitations of the state-of-the-art and contributions of this work.

1.1.1 Soft Error Trends in CMOS Technologies

Until the beginning of 1980s, the reports on soft errors were exclusively related to SEUs. The first results on SETs were published in 1983 by Diehl *et al.* [28], and the acronym SET was introduced in 1990 in the work of Newberry *et al.* [29]. In contrast to SEUs, which occur only in memory and sequential elements,

SETs can occur in combinational and memory/sequential elements, as well as in analog circuits and optoelectronic devices [30 - 32]. Thus, numerous publications refer to SETs in digital logic as Digital SETs (DSET) and to SETs in analog logic as Analog SETs (ASET). However, the focus of this work is only on SETs in combinational logic, and hence the acronym SET will be used.

The sensitivity of a logic cell, circuit or system to soft errors is typically expressed in terms of the rate of soft error occurrence, known as the Soft Error Rate (SER). The SER represents the number of soft errors in a given time interval, and it is determined as the sum of SER due to SEUs (sequential and memory SER) and SER due to SETs (combinational SER). The SER depends on irradiation conditions and a wide range of technology, design and operating parameters. The CMOS technology scaling trends have particularly strong impact on SER. For the choice of appropriate radiation hardening strategies in the IC design process, it is imperative to evaluate the impact of scaling trends on the cell-level and chip-level (system-level) SER, as well as the contribution of SETs and SEUs to the overall SER.

As technology scaling reduces the transistor size and supply voltage, individual transistors in a circuit become more sensitive to particle strikes in the sense that lower energy particles can induce SETs or SEUs. Conversely, smaller transistors have smaller sensitive area, and thus the probability that an incident particle will hit a sensitive transistor in a circuit decreases as technology scales down. Due to these competing scaling effects, and depending on the type of radiation, the cell-level SER has been either decreasing or increasing with the migration to a newer technology generation [33 - 39]. However, as the number of cells per chip increases with every new technology node, the **chip-level SER has been gradually increasing with technology scaling**, and this trend is also projected for the sub-10 nm technologies, as illustrated in Figure 1.2 [38]. Similarly, the SER of a complex system increases with the number of chips. As explained pictorially by Baumann [40], while a single chip may have the SER of one error in two years, a system with hundred chips may have the SER of one error per week.

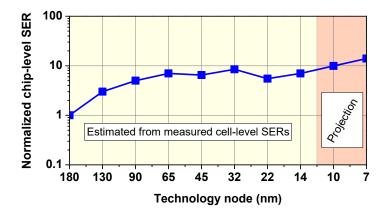


Figure 1. 2: Chip-level SER trends with technology scaling [38]

Concerning the contribution of SEUs versus SETs, numerous studies have confirmed that **SEUs are a dominant contributor to the overall SER** in all existing technologies. There are two main reasons for this. First, the largest part of a complex digital design, typically 50 - 90 % [41], is occupied by sequential logic and memory elements. Thus, the sensitive area of memory/sequential logic exposed to radiation is significantly larger compared to combinational logic. Second, it is very likely that a particle strike in an

unprotected sequential or memory element will cause a bit-flip because any amount of collected charge above the critical charge will flip the stored value. The memory elements such as Static Random Access Memory (SRAM) have lower critical charge than other logic gates due to smaller transistors, and are hence highly sensitive to soft errors. However, as the memory blocks can be efficiently hardened with error detection and correction logic, the sequential logic remains the main source of SEUs.

On the other hand, the probability that an SET pulse will cause a soft error is generally low because the SET propagation and latching are hindered by the inherent electrical, logical and temporal masking effects in logic circuits. Nevertheless, **the increase of clock frequency and the decrease of supply voltage, logic path length and propagation delay with technology downscaling have resulted in the increase of the SET contribution to the total SER.** The combinational SER increases linearly with clock frequency, while the sequential SER is almost frequency-independent [42, 43]. The contribution of SETs in logic circuits may be comparable or even exceed that of SEUs in flip-flops at clock frequencies in the order of several GHz [44]. Moreover, the reduction of supply voltage enhances the SET sensitivity, resulting in an increase of the SET contribution to the total SER [45 – 47]. In addition, the decrease of logic path length (number of combinational gates between two flip-flops) and propagation delay of combinational cells weakens the electrical and logical masking effects, enabling even very short SET pulses to propagate through the logic paths and eventually cause soft errors [48, 49].

In the light of the aforementioned technology scaling and SER trends depicted in Figure 1.1 and Figure 1.2, it can be expected that the soft errors will remain a critical reliability issue for the new technology generations. While there is still no evidence that SETs may dominate over SEUs in complex designs, the experimentally confirmed increase of SET contribution for different technologies suggests that the SETs are becoming more and more critical reliability factor. Thus, addressing the SET effects in mission- and safety-critical applications becomes imperative. However, despite the thorough research conducted by both academia and industry (over 1 million publications have been issued in the last 30 years according to Google Scholar), the inherent deficiencies of existing SET characterization, modeling and mitigation strategies impose the need for improved solutions which can more efficiently and cost-effectively address the SET effects in nanoscale CMOS designs.

1.1.2 A Soft-Error-Aware Design Concept

Due to the complex interplay of numerous contributing parameters, the design of rad-hard ICs is both challenging and expensive. The conventional rad-hard design approach based on standard cell libraries aims to minimize the system SER without violating the predefined design constraints regarding the area, delay and power consumption. To achieve cost-effective fault tolerance under variable radiation conditions, as for example in space, a rad-hard IC should feature the self-adaptive capabilities, such that the fault-tolerant mechanisms can be adapted autonomously to the changing radiation intensity. In that regard, in the soft-error-aware design it is necessary to address synergistically three main aspects (Figure 1.3):

• Soft error characterization and modeling: The SER of a target design is assessed in terms of relevant design, operating, technology and irradiation parameters. This is done with the computeraided simulations, employing various SET and SEU models at different levels of abstraction. The initial step is to characterize the SET/SEU sensitivity of the standard cell library, and these results are then used to compute the SER of the target design. To validate the simulation results and the soft error robustness of the final design, a limited number of irradiation experiments are conducted on manufactured chip prototypes.

- Soft error mitigation: As the standard cells are not sufficiently robust to soft errors, it is required to apply the soft error mitigation measures to reduce the SER. For environments with variable radiation exposure, the cost-effective approach is to combine the static and dynamic mitigation (fault-tolerant) mechanisms. Static mechanisms are continuously active during the runtime, while dynamic mechanisms can be adjusted as required. The mitigation is applied at multiple abstraction levels, and an optimal solution is chosen based on the sensitive elements identified during the soft error characterization process. The characterization and mitigation are performed iteratively until the minimum (or required) SER is achieved for the predefined design constraints.
- Online soft error monitoring: To enable the dynamic soft error mitigation under variable radiation conditions, the system needs to be aware of the impact of radiation intensity on its SER. This is achieved by monitoring the radiation intensity with appropriate particle detectors, thus enabling autonomous activation of mitigation mechanisms only when high radiation levels are detected. The monitoring is done by sensing either SETs or SEUs induced in the detector. The monitoring system needs to be more sensitive to radiation than the target design, and hence the characterization results for a specific technology are used as a reference in the design of soft error monitors.

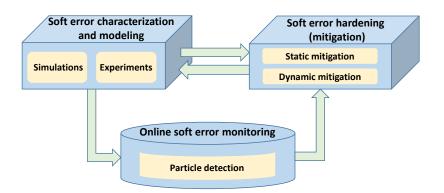


Figure 1. 3: Main elements of a soft-error-aware IC design concept

1.1.3 SET Characterization and Modeling

To determine the SER of a combinational circuit and select the most appropriate SET mitigation strategy, it is necessary to quantify the SET sensitivity of each gate in the circuit, i.e. to evaluate the contribution of each gate in terms of its impact on the SET generation and propagation. Because of the analog nature of SET pulses, a wide variety of combinational cells in a digital library, and heterogeneity of combinational circuits, the SET effects are more difficult to characterize than SEUs [50]. The most reliable approach to assess the SER of a given design is through the accelerated irradiation experiments (e.g with heavy ions). However, such experiments are expensive (around 20 000 Euro per experiment), require a manufactured chip, and provide very limited information on the sensitivity of individual cells in the design. A cheaper alternative are the laser experiments which can be conducted in-house and allow to assess the sensitivity of

individual cells, but this approach also requires a chip prototype. Hence, the standard methodology for evaluation of SET effects in the early design phases relies on the multi-level computer-based simulations, while the heavy ion and/or laser experiments are used in the final design and verification phases.

Conducting the simulations for every gate in a complex circuit and all parameters affecting the SET response requires extreme effort in terms of time and resources. The SET characterization usually combines simulations and analytical methods, and is performed in two phases: (i) characterization of standard cell library through simulations, and (ii) analytical evaluation of the SER of a target design. Although numerous SET characterization methodologies and analytical models have been proposed, the common limitations are the **insufficiently accurate models** and **computationally intensive characterization process** for large standard libraries and target designs with a large number of inputs and outputs. The standard library is characterized with extensive simulations for every cell, and the simulation results are stored in look-up tables (LUT). Although this procedure is done once, it may be very time-consuming if performed for all possible combinations of contributing parameters. The characterization LUTs and analytical models for SET effects are employed to analyze the target circuit instead of performing the simulations for every node in the circuit. However, the use of raw characterization results in subsequent SER computation is timeconsuming because of the need to access and read a huge amount of data stored in LUTs. The existing SET models have insufficient accuracy because they often neglect some important effects in order to simplify the analysis. Furthermore, the analytical evaluation methods suffer from the scalability issues, which limits their overall effectiveness. Therefore, for fast and efficient SET characterization it is necessary to optimize the characterization process and improve the accuracy of used models. More details on the limitations of existing SET modeling and characterization approaches are presented in Chapter 3.

1.1.4 Radiation Hardening Techniques

A wide range of hardening techniques can be applied to reduce the SER of a given design. In general, the radiation hardening techniques are classified into three distinct approaches:

- *Radiation Hardening by Shielding (RHBS)*: The RHBS consists in adding a sheet of metal around the target device or using specially-designed packages. This approach may stop or attenuate low energy particles, but it is not affective against high energy ions and neutrons [51].
- *Radiation Hardening by Process (RHBP)*: The RHBP includes the measures applied in the manufacturing process, either by using special materials or modifying the technology. For example, the recent Silicon-on-Insulator (SOI) and Fin Field Effect Transistor (FinFET) processes have shown improved radiation hardness over planar CMOS [37, 39].
- *Radiation Hardening by Design (RHBD)*: The RHBD techniques are related to the modification of original design in order to mitigate the radiation effects. This can be accomplished with hardware (spatial), software, temporal or information redundancy, or some combination of them [52].

Among the three aforementioned radiation-hardening styles, the RHBD is the most common since it can be adapted to an existing non-rad-hard technology, providing high-level of soft error robustness with lower cost compared to RHBP. The RHBD techniques offer the flexibility from the implementation perspective as they can be implemented either as static or dynamic, at multiple levels of abstraction (gate, circuit and system levels). The standard approach for reducing the SER of combinational logic is the Triple Modular Redundancy (TMR), originally proposed by Neumann in 1958 [53]. However, TMR introduces very high area, performance and power penalties, and is therefore not suitable for cost-constrained applications. Since the sensitivity of logic gates in a circuit is non-uniform, the cost-effective SER reduction can be achieved with the selective gate-level hardening, i.e. by hardening only a limited number of the most sensitive logic gates [54]. Then, if the required SER cannot be achieved, the gate-level hardening can be complemented with the circuit- and system-level hardening techniques.

The gate-level SET mitigation can be accomplished by: (i) redesign of the cell structure, or (ii) replacing a sensitive cell with a more robust cell from the same library, or adding redundant logic to an existing cell. Because it does not require to modify the existing cells, the later approach is widely accepted. A detailed review of the most common hardening techniques for standard cells is given in Section 3.4. Individual techniques provide only limited improvement of SET robustness (by addressing dominantly either the SET generation or the SET propagation effects), at the cost of area, delay and power overhead. As a result, the effective **SET mitigation requires to use multiple techniques**. However, there is no an optimal approach for combined gate-level mitigation. Furthermore, **characterization of the gate-level mitigation solutions for every new design requires additional simulation and analysis effort, which increases the SER evaluation runtime**. These limitations impose the need for alternative gate-level SET mitigation solutions, as well as for comprehensive characterization of gate-level techniques in order to quantify their impact on individual standard cells.

1.1.5 Online Soft Error Rate Monitoring

Because of variable intensity of space radiation, the SER of an electronic system may vary by several orders of magnitude over a period of few hours or days. In such cases the soft error mitigation based exclusively on static techniques would lead to high penalties (excessive power consumption), which is critical in long-term missions due to the limited power resources. To overcome this issue, the selective gate-level and/or circuit-level static mitigation solutions are complemented with the dynamic mitigation solutions applied at the system level. To enable dynamic activation of mitigation mechanisms, the radiation intensity should be monitored continuously during the mission. In such a way, the optimal trade-off between performance, power consumption and radiation hardness can be maintained in real time. A typical approach is based on the self-adaptive processing systems, where the operating and fault-tolerant modes are selected according to the radiation conditions and application requirements [55 - 58].

The detection of radiation particles responsible for the soft errors is performed with special hardware sensors. In order to assess the impact of both SETs and SEUs, the monitoring of both flux and Linear Energy Transfer (LET) of incident particles is required. Various particle detection techniques have been proposed in literature, and a detailed overview is given in Section 3.5. The particle detectors operate on the principle of detecting the rate of SETs or SEUs, and from this information the particle flux and LET can be determined. However, the existing solutions have at least one of the following drawbacks: (i) **cannot measure both the particle flux and LET**, (ii) **require highly complex and costly processing logic**, (iii) **not suitable for on-chip integration with the target system**, (iv) **may produce erroneous response due to false alarms, multiple errors and accumulation of errors**. As a consequence, there is a need for low

complexity and cost-effective online soft error monitoring solutions, which can sense the variation of both particle flux and LET, allowing for the systematic real-time assessment of the contribution of SETs and SEUs to the system SER.

1.2 Research Scope and Objectives

This work was conducted in the framework of project REDOX (*Reduction of Simulations and Irradiation Experiments by Optimization of SET Effects Evaluation*), funded by the German Research Foundation DFG (*Deutsche Forschungsgemeinschaft*). The primary goal of this research is to enhance the characterization, modeling and mitigation of SET effects in standard combinational cells. Considering the general soft-error-aware design concept illustrated in Figure 1.3 and the limitations of the state-of-the-art outlined in previous discussion, the following objectives have been defined:

<u>Objective 1:</u> To optimize the characterization of SET effects in standard combinational cells, and enhance the models for predictive analysis of SET generation and propagation effects

Given that the simulation-based SET characterization may be very time-consuming due to the necessity to consider a large number of dependencies, the characterization of a standard library has to be optimized by reducing the total characterization time. To achieve this, the number of simulations for each standard cell need to be reduced. In order not to compromise the accuracy of the characterization results, the reduction of simulations should be done by exploiting the inherent similarities in the SET response of the standard cells. In addition, the total amount of characterization data and the runtime of the subsequent SER analysis of a given design must be also minimized. In that regard, the accurate analytical models for predictive analysis of the SET sensitivity are required. To obtain the models that can be easily integrated in a standard digital design flow, the modeling approach based on fitting of characterization results can be used. By introducing the predictive models with improved accuracy (taking into account some essential parameters that are neglected in the existing models), the characterization database can be significantly reduced, thus enabling to speed up the characterization of SET effects in a target circuit or system.

<u>Objective 2:</u> To improve the SET robustness of standard combinational cells by exploring new cost-effective solutions, and quantify the benefits and limitations of existing techniques in order to facilitate the combined application of multiple techniques

Due to the lack of a unified gate-level SET mitigation methodology, and the inherent deficiencies of existing techniques, it is important to explore alternative solutions that can improve the SET robustness of standard cells with lower area, delay and power overheads compared to existing techniques. As the goal is to preserve the existing standard cell designs, a possible solution is in selecting appropriate redundant configuration(s) that can be connected to the output of standard cells to increase the critical charge and SET filtering capability. In addition, to exploit the unique advantages of different hardening approaches, it is necessary to combine multiple techniques for selective hardening of the most sensitive nodes in the design. For cost-effective combined application of gate-level techniques in a given design, it is necessary to characterize the quantitative impact on SET generation and propagation resulting from the application of each technique, as well as the introduced area, power and delay overhead per gate.

<u>Objective 3:</u> To enhance the on-line SER monitoring by enabling the measurement of both particle flux and LET, based on a low cost purely digital readout

As the system SER is strongly influenced by particle flux and LET, the on-chip detector(s) should provide the information on both parameters to allow for accurate computation of SER variations. This information can then be used for triggering the dynamic fault tolerance mechanisms in the system. To address the performance limitations as well as complexity and cost issues of the existing soft error monitoring solutions, we aim to investigate the online SET monitoring as a possible alternative. As the combinational logic is not prone to error accumulation, using custom-designed combinational logic as a particle detector may provide significant performance and cost gains over existing particle detection solutions. In addition, to reduce the cost of implementation and performance overheads, we aim to investigate the feasibility of purely digital processing logic, with low power consumption and fast response (low detection latency).

1.3 Thesis Contributions

In order to address the presented research challenges, we propose a methodology that combines the characterization of the SET sensitivity of standard combinational cells and the respective static gate-level hardening configurations applicable to standard cells. Additionally, to support the dynamic soft error mitigation, we propose an approach for detection of energetic particles based on SET sensing. Specifically, the following are the main contributions:

- 1. A holistic approach for characterization of SET effects in standard combinational cells and respective gate-level hardening configurations, with reduced number of simulations and reduced SET sensitivity database. The proposed approach is based on the characterization of SET effects in standard cells using two current sources in SPICE simulations [MA4, MA6, MA10, MA11, MA12, MA19]. By characterizing jointly the standard cells and the gate-level hardening configurations, a unified SET sensitivity database for a given standard cell library can be established. We have shown that the inherent similarities in the SET response of multi-input logic gates can be exploited to reduce the number of simulations during characterization [MA10]. To the best of our knowledge, we have demonstrated for the first time that the standard delay cells based on skew-sized inverters are the most SET-sensitive standard cells [MA19]. In addition, we have shown that the total amount of data can be reduced by deriving the analytical models for SET sensitivity from the simulation data, and then storing the model fitting coefficients in LUTs instead of raw simulation data [MA15]. As the number of fitting coefficients is far less than the number of simulation data, the total number of characterization values in LUTs can be reduced by several orders of magnitude. Based on characterization results, we have proposed a generic format for the model-based SET sensitivity LUTs.
- 2. Analytical models for SET generation and propagation metrics (critical charge, generated SET pulse width and propagated SET pulse width) based on the superposition principle and fitting of results from SPICE simulations. By addressing some of the key limitations of existing models, we have derived alternative models for predictive analysis of critical charge, generated SET pulse width and propagated SET pulse width [MA1, MA5, MA9, MA14, MA15]. The proposed models represent the SET sensitivity metrics as a function of the sum of contributing parameters. Compared

to existing models, our modeling approach offers the following benefits: (i) possibility to identify the contribution of individual parameters, (ii) only the parameters which are essential in the design phase are considered, while the technological parameters are transparent to the designer, (iii) the impact of additional parameters not considered by the existing models is taken into account. It is particularly important to note that the proposed SET pulse width model has been derived using an existing bias-dependent current source, providing higher accuracy in estimation of SET pulse width compared to the standard models based on widely used double-exponential current model.

- **3.** A gate-level SET mitigation approach based on insertion of decoupling cells at the output of a logic gate. We have demonstrated for the first time that the insertion of two decoupling cells at the output of a combinational gate improves its robustness to particle strikes (due to the increase of critical charge of the gate's output node), and enhances the attenuation of short SET pulses [MA13]. Each decoupling cell consists of two cross-coupled NMOS and PMOS transistors, and increasing the size of transistors provides a better SET robustness. The advantage with respect to the most common gate-level mitigation techniques (gate sizing and gate duplication) is better SET filtering. In comparison with techniques based on insertion of redundant logic, our approach can provide higher robustness to SET generation (larger increase in critical charge).
- 4. A comparative characterization of proposed SET mitigation technique with decoupling cells and seven existing techniques, through a quantitative assessment of their impact on the improvement of SET robustness of individual logic gates. Using our initial results [MA13] as a reference, we have conducted a detailed characterization to quantify the critical charge, generated SET pulse width and propagated SET pulse width, when each of the considered techniques are applied to standard cells. We have shown that the analyzed techniques have differing impact on standard cells, i.e., some techniques are effective only for certain logic gates. In addition, we have demonstrated that at least two techniques are required for SET suppression in a combinational path. Accordingly, the guidelines for the application of each technique have been defined.
- 5. A particle detector based on skew-sized pulse stretching inverters for the on-line monitoring of particle flux and LET variations. We have shown for the first time that, besides its applicability for the SET pulse width measurement [MA2, MA7, MA8], the pulse stretching feature of skew-sized inverters can be also exploited for detection of energetic particles [MA16]. Using specially designed pulse stretching inverters enables to monitor the particle flux in terms of SET count rate, and to sense the LET variations by sorting the detected SETs in several pulse width ranges [MA3, MA17, MA18]. The advantages over the existing detectors are the possibility to monitor both the particle flux and LET variations with purely digital processing logic featuring low detection latency and power consumption, and immunity to false alarms and multiple errors. The solution offers a high level of flexibility, as it can be implemented either as a stand-alone detector or integrated in the target chip.

The contributions of this work may serve as a basis for establishing a comprehensive multi-level radhard design flow, which integrates the characterization, hardening and online soft error monitoring. The characterization database for the standard cell library and the SET sensitivity models are essential for the analytical SER analysis of a complex design. In that way, the need for fault injection in every circuit node of the target design can be minimized or even eliminated. Similarly, the characterization database for gatelevel hardening configurations can be used as a guideline in selection of an optimal strategy for the selective gate-level SET mitigation, as the preliminary phase in the hardening of combinational circuits. Finally, the on-line particle detection serves as a key enabler of the adaptive fault tolerance in ICs employed in long-term space missions. As a proof of concept, the analysis was mostly done for the IHP's 130 nm bulk CMOS technology. This technology is a part of IHP's commercial space-grade SiGe BICMOS platform. Besides the 130 nm technology, a part of analysis was done with IHP's 250 nm and UMC's 65 nm bulk CMOS technologies.

1.4 Thesis Organization

The rest of the thesis is organized into six chapters, as follows:

In **Chapter 2**, the fundamental aspects of SET effects in CMOS technologies are discussed. The typical radiation sources and related physical quantities are briefly introduced. This is followed by the discussion of the SET generation and propagation mechanisms, and the metrics for evaluation of the SET sensitivity. Furthermore, the effects of technology scaling on the SET sensitivity are discussed based on published experimental results. Finally, the impact of design, technology, operating and irradiation parameters on the SET sensitivity are elaborated.

Chapter 3 reviews the state-of-the-art in the three main topics addressed in this thesis: (i) characterization and modeling of SET generation and propagation effects in standard combinational cells, (ii) gate-level SET mitigation techniques, and (iii) particle detection for online SER monitoring. For each of these topics, the most significant state-of-the-art achievements are summarized, and the open issues addressed in this thesis are outlined.

Chapter 4 deals with the characterization and modeling of SET effects in a standard cell library. First, a methodology for the SPICE-based characterization of SET effects in standard combinational cells and respective gate-level hardening configurations, is introduced. Next, a detailed characterization of the critical charge, generated SET pulse width and propagated SET pulse width in terms of key contributing parameters, for the most common standard cells, is presented. Based on the characterization results, a set of design guidelines is proposed. By fitting the simulation results, the analytical models for critical charge, generated SET pulse width and propagated SET pulse width are derived. The applicability of the proposed models to two application-specific standard cells is evaluated. The analysis of the possible reduction of the number of simulations and the output SET database is then presented. The chapter concludes with the summary of achieved results and outline of issues to be addressed in future work.

Chapter 5 addresses the SET mitigation in standard combinational cells. First, the use of decoupling cells for SET mitigation is discussed. The proposed technique is characterized by employing the methodology introduced in Chapter 4. Similar approach is then applied to comparatively analyze the proposed technique and seven existing techniques in terms of SET robustness improvement and respective area, delay and power overheads. An example of the combined application of multiple techniques for SET mitigation in a logic chain is presented. As a special case study, the SET mitigation in standard delay cells is analyzed. Based on obtained results, the benefits and limitations of each technique and a brief guideline for the choice of each technique are given. The chapter is concluded with the outline of directions for future research.

Chapter 6 introduces the custom-sized pulse stretching inverters as particle detectors for triggering the dynamic fault tolerance. The design and normal operation of a two-inverter pulse stretching cell is initially presented. Then, the use of a single pulse stretching cell for detection of energetic particles in terms of induced SET pulses, and the configurations based on serial and parallel connection of pulse stretching cells, are analyzed with SPICE simulations. A conceptual design of the readout logic for the serial and parallel configurations is presented. The proposed solution is then compared with the existing particle detectors in terms of design and performance metrics. An example of application in a self-adaptive multiprocessing system is given. The summary of achieved results and possible follow-up work conclude the chapter.

Finally, **Chapter 7** summarizes the most important results presented in the thesis, and outlines the main strategic directions for future work.

1.5 Publications

Most of the results presented in this thesis have been published in peer-reviewed journals and at national and international conferences, as follows:

Journal publications:

- [MA1] M. Andjelkovic, V. Petrovic, Z. Stamenkovic, G. Ristic, G. Jovanovic, "Circuit-level Simulation of the Single Event Transients in an On-chip Single Event Latchup Protection Switch," *Journal* of Electronic Testing - Theory and Applications, vol. 31, pp. 275 – 289, 2015.
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The author of this work has also co-authored 2 journal papers and 5 conference papers partly related to the topics investigated in this work. These publications are listed in the Bibliography as references [58], [140], [159], [232], [278], [295], and [296].

Chapter 2

Basics of SET Effects

Understanding the physical and electrical aspects of the Single Event Transient (SET) effects and the impact of various parameters on the SET sensitivity is crucial for the analysis of SET effects in digital circuits and the design of rad-hard circuits and systems. In that regard, this chapter introduces the basics of the SET effects in CMOS combinational logic. The chapter is divided into six sections. Section 2.1 gives a brief description of space and terrestrial radiation environments, and main physical quantities for assessing the interaction of radiation particles with semiconductors. The SET generation and propagation mechanisms are described in Sections 2.2 and 2.3, respectively. Section 2.4 outlines the key metrics for SET sensitivity assessment. In Section 2.5, the impact of technology scaling trends on the SET sensitivity is elaborated. Finally, Section 2.6 discusses the dependence of SET sensitivity on technology, design, operating and irradiation parameters, as well as the combined impact of multiple parameters, which is essential for the accurate SET characterization and modeling.

2.1 Radiation Environments and Quantities

The energetic particles that are primarily responsible for soft errors in space are neutrons, protons and heavy ions. These particles originate from three sources: galactic cosmic rays from deep space, Solar Particle Events (SPEs) resulting from solar flares and coronal mass ejections on the Sun, and particles trapped in the Earth's magnetic field (Van Allen belts). In scaled (sub-100 nm) technologies, the electrons and muons may also cause the soft errors [59 – 62]. The alpha particles emitted from the chip packaging materials have been a major cause of soft errors for a long time, but this has been alleviated by employing the low-alpha-emitting materials. At terrestrial level, the energetic particles can be encountered either as atmospheric neutrons and muons originating from the interaction of cosmic radiation with the atmosphere, or as man-made radiation sources employed in various applications in research, industry and medicine. A detailed description of space and terrestrial radiation can be found in [63 - 66].

While the man-made radiation sources are usually employed in well-controlled conditions, the natural radiation produces variable and often unpredictable exposure rates, and therefore poses significant risk to the functionality of electronics employed in such environments. Due to its complexity and dynamic nature, the space radiation is more dangerous for electronics than the ground-level radiation. The intensity of

radiation exposure in space may vary significantly over a short period of time. For example, during an SPE the radiation intensity may increase by 2 - 5 orders of magnitude above the background level, and this condition may last for several hours or days [67, 68]. The energy of particle radiation covers a range from meV up to GeV. The exposure rate (radiation intensity), is expressed in flux and fluence. Flux denotes the number of particles passing through a unit area per unit time, and it is measured in particles/cm²/s. Fluence is the number of particles per area, expressed in particles/cm². The flux and fluence depend on the altitude, location and dynamics of the radiation environment (solar cycle).

The interaction of a single particle with the target material is characterized by the Linear Energy Transfer (LET) and the particle's track length in material. LET denotes the energy lost by a particle per unit track length, normalized by the density of the target material, and it is expressed in MeV·cm²·mg⁻¹. In space, **the low-LET particles are more abundant that the high-LET particles,** and the particles with LET above 30 MeV·cm²·mg⁻¹ are rare [69]. The value of LET is considered to be independent of material properties due to the normalization with the target material density. However, LET varies with the distance the particle travels through the target material, resulting in non-uniform charge deposition. The dependence of LET on particle's track length is described with the Bragg's curve [70, 71]. For the sake of simplicity, it is often assumed that LET is constant along the particle's track. The particle's track length in silicon depends on the type of particle, and it ranges from several µm to hundreds of µm.

2.2 SET Generation Mechanisms

An SET occurs when an energetic particle passes through the sensitive region of a transistor within a combinational gate. The passage of an energetic particle through a semiconductor device and the creation of an SET pulse involves two main physical mechanisms: **charge generation** and **charge collection**. As a result of these mechanisms, the SET current pulse is induced in the device, and eventually transformed into the SET voltage pulse (glitch). If the SET voltage pulse propagates through a combinational path and is captured by a storage element, a soft error occurs.

2.2.1 Charge Generation

When an energetic particle passes through a semiconductor material, it loses energy along its path. As a result, the free charge carriers (electron-hole pairs) are released within the material. The amount of charge Q_{GEN} (in pC) generated in a specific material as a result of particle strike is defined by the particle's LET (in MeV·cm²·mg⁻¹) and track length *l* (in µm), and for silicon it can be expressed as [72, 73],

$$Q_{GEN} = 1.035 \times 10^{-2} \times l \times LET \tag{2.1}$$

The charge generation in semiconductor devices is governed by two ionization mechanisms: *direct ionization* and *indirect ionization* [70]. Direct ionization occurs when an ionizing particle passes through a semiconductor device and collides with the electrons, resulting in immediate creation of charge (electronhole pairs) along the particle's track. This process is caused mainly by heavy ions, electrons and alpha particles. In order for direct ionization to occur, the energy transferred by the incident particle must be larger than the ionization energy of the target material (for silicon the ionization energy is 3.6 eV). Indirect

ionization is typically caused by protons and neutrons. When protons or neutrons pass through a semiconductor material, they collide with the nuclei in the material, initiating nuclear reactions which result in secondary ionizing particles such as heavy ions. The created secondary ionizing particles then deposit the charge through direct ionization.

2.2.2 Charge Collection

The passage of an energetic particle through a typical CMOS device is illustrated in Figure 2.1. Most of the charge carriers released in the substrate region will eventually recombine, producing no effect on the circuit response. However, the charge generated within and near the p-n junctions will be collected by the internal electric field and transformed into pulsed (transient) current [70]. The most sensitive regions in a CMOS circuit are the depletion layers across the reverse biased p-n junctions in PMOS and NMOS transistors [70, 74]. This means that **the off-state transistors are most sensitive to particle strikes, while the on-state transistors act as restoring elements**, i.e., provide the current to compensate the particle-induced current and restore the previous logic state. The three main charge collection mechanisms in CMOS devices are [70]: *drift, funneling,* and *diffusion*.

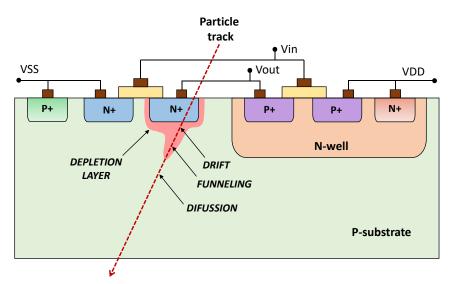


Figure 2.1: Basic mechanisms of particle interaction with a *p-n* junction in CMOS inverter

Drift mechanism is responsible for charge collection within the depletion layer, where the intensity of the electric field is strongest. If the deposited charge exceeds the doping concentration, the depletion region may be temporarily distorted and extended down into the substrate. This extended depletion region is known as a funnel, and the charge collection within this region is referred to as the funneling collection. The funneling effect is typical in low-doped substrates, and it is caused by high-LET particles. As a result of the difference in charge concentration within the device, the charge outside of depletion region, but within the diffusion length of charge carriers, may be collected through the diffusion process. The drift and funneling are fast processes (lasting for hundreds of picoseconds), and they are responsible for the SET initiation. On the other hand, the diffusion is a slow process (lasting for nanoseconds to microseconds), and it defines the recovery of the device (restoration of previous logic state).

Besides the three main charge collection mechanisms, the particle-induced charge may be also collected through two additional mechanisms: *parasitic bipolar amplification* and *alpha particle source-drain pene-tration (ALPEN)*. Both of these effects are common in scaled technologies. The source-drain-well region of the NMOS (PMOS) transistors acts as a parasitic *n-p-n* (*p-n-p*) bipolar transistor. If the deposited charge triggers this parasitic bipolar structure, the charge collection is enhanced and significantly larger amount of charge may be collected. As a result of charge collection amplification, multiple transistors may collect the induced charge [75]. On the other hand, the ALPEN effect occurs when a particle passes simultaneously through both drain and source of a transistor, and also results in the collection of significant amount of charge. This may happen in the case of near-grazing incidence, i.e., when a particle traverses the device at very small incidence angle [76].

2.2.3 SET Current and Voltage Pulse Formation

As a consequence of the particle-induced SET current, the SET voltage pulse may be generated at the output of a target logic gate. The electrical response of a CMOS circuit to a particle strike is illustrated in Figure 2.2, using an inverter as example.

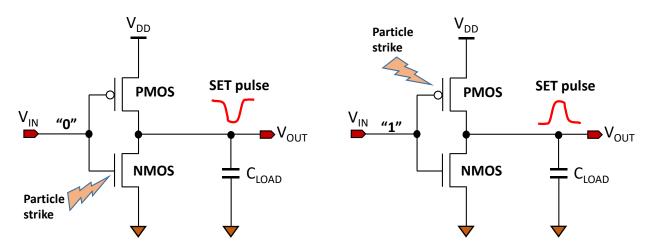


Figure 2.2: Effect of particle strike in an inverter for low (0) and high (1) input levels

Assuming a low level at the input of inverter, the sensitive transistor is the off-state NMOS transistor. When a particle strikes the NMOS transistor, the on-state PMOS transistor and load will provide the current to counteract the induced current and restore the initial logic state. The maximum current that can be supplied by the restoring on-state transistor is equal to its drive current. However, if the induced charge exceeds the charge stored in the hit node, an SET voltage pulse will be formed. This voltage pulse lasts until the induced current is drawn away through the restoring (on-state) transistor. The situation is similar for the high-level input, whereby the sensitive transistor is PMOS and the restoring transistor is NMOS. Due to different characteristics of PMOS and NMOS transistors, the resulting current and voltage pulse shapes due to hits in PMOS and NMOS transistors will differ.

The amount of collected charge, and thus the current pulse shape, is a complex function of technology parameters (doping concentration and charge collection volume), radiation parameters (LET, angle of

incidence and strike location), supply voltage and load. In general, the SET current pulse may have the amplitude from hundreds of nA to several mA. The most common shape of the SET current pulse has a short rising edge and a long falling edge, as depicted in Figure 2.3 (a). This current pulse is known as the double-exponential current pulse because it can be mathematically modeled with a double-exponential function (as will be explained in Section 3.3.1). When a particle passes directly through the drain, the drift collection is dominant and the current pulse has high amplitude and small width. Otherwise, when a particle passes away from the drain, the diffusion process dominates and the current pulse has smaller amplitude and larger width. The amount of collected charge may be also increased due to angular strikes, which have longer trajectories and produce more charge than particles traversing at normal incidence.

However, the shape of the current pulse may deviate from the illustrated double-exponential shape if the induced current exceeds the driving current of the restoring transistor, which may happen when the particle has high LET. In that case, the current pulse will have a short peak and a long plateau region as illustrated in Figure 2.3 (b). The amplitude of the plateau is equivalent to the driving current of the restoring transistor, while the duration of the plateau increases with the particle LET. It was demonstrated with device simulations for 90 and 130 nm CMOS technologies that the current pulse has the double-exponential shape for LET < 10 MeV·cm²·mg⁻¹ and the plateau-like shape for higher LET values [77].

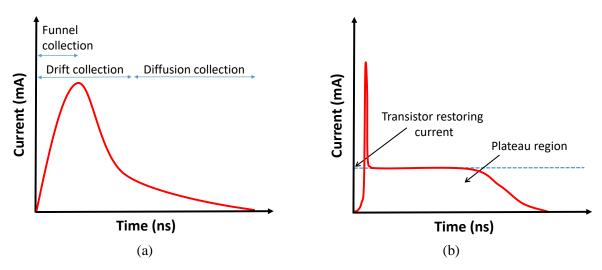


Figure 2.3: Typical shape of SET current pulse (not to scale) for: (a) low LET, and (b) high LET

The SET voltage pulse resulting from the induced current is analog in nature, and it is characterized by three parameters: amplitude, duration and polarity. The amplitude of the SET voltage pulse may have any value between ground and supply rails, while the **SET pulse width is typically in the range from tens of ps to several ns** [78]. The SET pulse can have positive polarity (0-to-1 pulse) or negative polarity (1-to-0 pulse), where the polarity depends on the logic state of the target gate. If the output of a target gate is at low level (logic 0), the induced SET would have positive polarity. Conversely, if the output is at high level (logic 1), the SET will have negative polarity. A typical shape of the SET voltage pulse with positive polarity, for different LET, is illustrated in Figure 2.4. The SET pulse width increases monotonically with LET, but it is also dependent on strike location and angle of incidence, as well as design and operating parameters, as will be discussed in Section 2.6. It is important to note that the SET pulse width would not

be constant for a given LET, but rather a distribution of SET pulse widths will be obtained, because of the random strike locations and incidence angles. As a consequence, the variability of SET pulse width for a combinational chain may be in the range of tens to hundreds of picoseconds for a given LET.

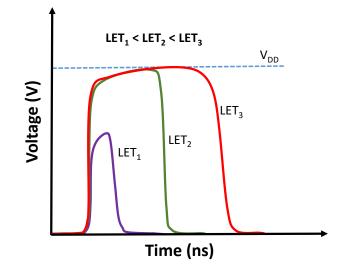


Figure 2.4: Typical shapes of positive (0-to-1) SET pulse for different LET

2.2.4 Charge Sharing and Single Event Multiple Transients

In older CMOS technologies, a single particle strike would result in the charge collection within a single transistor. However, as the transistors are becoming smaller with technology downscaling, and the spacing between transistors is reduced, it has become possible that a single particle deposits charge within two or more transistors located at close proximity. The effect of simultaneous charge collection by two or more transistors is known as *charge sharing*, and it typically occurs in technologies below 250 nm [79, 80]. This effect is also referred to as the *Multiple Node Charge Collection (MNCC)* [81]. The charge sharing may occur if the diameter of the particle's track is larger than the transistor size, in the case of angular strikes, or due to parasitic bipolar amplification. The particles with higher LET (energy) create wider charge track, and are more likely to deposit charge in multiple nodes. For example, Ebrahimi *et al.* have shown that a particle with energy of 22 MeV may affect the area of around 1.2 μ m², while a particle with energy of 144 MeV may affect the area of 4.6 μ m² [82]. Based on irradiation experiments on 65 nm technology, Harada *et al.* have observed that a single particle may hit up to six adjacent inverters [83], while Zhang *et al.* [84] have demonstrated that up to five inverters may be hit simultaneously in the case of angular strikes.

If a single particle causes the charge collection in two or more combinational gates which are not electrically connected, two or more independent SETs may be generated. This effect is known as the *Single Event Multiple Transients (SEMT)* [85]. As the transistor dimensions decrease and the packing density increases, the probability of *SEMTs* rapidly increases. Multiple SETs propagating through independent logic paths may result in multiple soft errors. However, the charge sharing may also lead to a beneficial effect known as *pulse quenching*, which results in the reduction of SET pulse width. This effect was first discovered in 2009 by Ahlbin *et al.* [86], at the 130 nm node, and it occurs when the charge is collected by two electrically connected gates which cause the inversion of signal polarity.

2.3 SET Propagation Mechanisms

The SET pulse generated at the output of a logic gate can cause a soft error only if it propagates through a combinational path and is eventually captured by a storage element. In order for this to happen, the following conditions must be met:

- The amplitude and width of SET pulse must be sufficiently large.
- A sensitized logic path must exist between a target gate and a storage element.
- The SET pulse must arrive at the input of a storage element within the latching window.

Depending on various propagation-induced effects, four main SET propagation scenarios are possible: (i) SET pulse is broadened during propagation, (ii) SET pulse is attenuated during propagation, (iii) SET pulse is converted into multiple SETs, and (iv) SET pulse is filtered (masked).

2.3.1 SET Masking Effects

The three main effects which can hinder the propagation of SETs through a combinational path are: *electrical masking, logical masking* and *temporal masking* [48, 67]. Figure 2.5 illustrates the masking effects in a simple circuit.

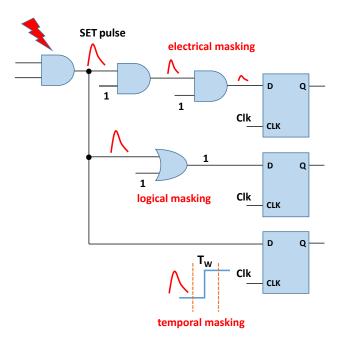


Figure 2.5: Effect of electrical, logical and temporal masking on SET propagation

(a) Electrical masking

Electrical masking occurs if the SET pulse is attenuated and eventually filtered by the subsequent gates in a logic path. All logic gates act as inherent low pass filters due to their capacitance and limited slew rate, and therefore can potentially attenuate the SET pulses. The amplitude and width of the SET pulse and the propagation delay of subsequent logic gates are the primary factors affecting the electrical attenuation. For

example, XOR and XNOR gates have larger propagation delay than inverters, and therefore cause stronger SET attenuation. The SET pulses wider than the propagation delay of subsequent gates will propagate with minimum or no attenuation, while the short SET pulses are likely to be filtered. In other words, the electrical masking probability is inversely proportional to the SET pulse width.

(b) Logical masking

Logical masking occurs when at least one input of a logic gate is set to controlling value. In that case, the output of the gate will be determined by the controlling value of the input, and an SET pulse will not propagate. Typical examples of gates with logical masking capability are AND, NAND, OR, NOR. For example, if one input of AND gate is at logic 0, its output will be at logic 0, and any SET that arrives on the other input will be masked. On the other hand, INV, BUF, XOR and XNOR gates do not have logical masking capability. The probability of logical masking depends on the logic operation of the circuit and input logic vectors, but not on electrical or technological parameters. In general, the combinational paths with a larger number of gates with controlling inputs are more likely to cause logical masking.

(c) Temporal masking

Temporal masking (also known as timing masking or latching-window masking) occurs when an SET pulse reaches a flip-flop, but not within the latching-window interval during which the flip-flop can capture the input signal. The temporal masking probability is determined by the SET pulse width, setup and hold times of the flip-flop, clock frequency and instant when the SET arrives at the input of flip-flop. In order to be latched by a flip-flop, the SET pulse should be wider than the sum of setup and hold times of the respective flip-flop. The latching probability increases linearly with the SET pulse width, and also with the clock frequency, because at higher frequency more clock edges are available to capture the SET pulses.

2.3.2 Other SET Propagation Effects

Apart from being electrically masked, an SET pulse may be broadened during propagation through a logic path. This effect is known as the Propagation-Induced Pulse Broadening (PIPB), and it was first observed in 2007 by Ferlet-Cavrois *et al.* [87]. The magnitude of pulse broadening is determined by the type, size and number of gates in the path, input logic levels, supply voltage and SET polarity [87 - 90]. Depending on the composition of a logic chain, the SET pulse can be broadened from several ps to tens ps per gate [86, 88, 89]. For example, the heavy ion experiments have shown that an SET pulse of 200 ps is broadened to almost 2 ns after passing through a chain of 800 inverters in 130 nm SOI CMOS technology [87].

Besides the PIPB effect, the SET pulse propagation can be affected by the reconvergent paths, which are very common in large combinational circuits such as arithmetic circuits. Depending on propagation delay of reconverging paths, an SET pulse path may be shrunk, broadened, converted into multiple SETs or filtered. The SET pulse can be also broadened or filtered during propagation through a logic path composed of skew-sized cells. Moreover, a single SET pulse can be turned into multiple SETs when it propagates through diverging paths such as those in clock and reset trees, potentially resulting in multiple soft errors. In scaled technologies, due to reduced spacing between the interconnections, the SETs can produce crosstalk effect on neighboring lines and result in the change of logic level [91, 92].

2.4 SET Sensitivity Metrics

Various metrics are employed for quantifying the soft error sensitivity of a gate, circuit or system, as well as for assessing the effectiveness of the soft error mitigation solutions. The common sensitivity metrics are: critical charge (threshold LET), SET pulse amplitude/width, soft error rate, and cross-section.

2.4.1 Critical Charge (QCRIT) and Threshold LET (LETTH)

The critical charge (Q_{CRIT}) denotes the minimum collected charge required to alter the corresponding logic level [93, 94]. It is a measure of the sensitivity of a single circuit node (transistor). Lower values of critical charge indicate higher SET sensitivity. For combinational gates, Q_{CRIT} is defined as "the minimum collected charge that results in an SET voltage pulse with amplitude beyond the threshold level (half of supply voltage)". The Q_{CRIT} is an essential figure of merit for estimation of the SET generation probability, i.e., the nominal SER, as will be explained in Section 2.4.3. The typical values of Q_{CRIT} range from several fC to hundreds of fC. The value of Q_{CRIT} for a given circuit node is not constant but depends on numerous factors, as will be explained in Section 2.6.

The threshold LET (LET_{TH}) is analogous metric to Q_{CRIT} and is defined as the minimum LET required to cause an SET pulse with amplitude beyond the threshold level. Based on equation (2.1), the relation between LET_{TH} and Q_{CRIT} can be approximated as,

$$Q_{CRIT} = 1.035 \times 10^{-2} \times L \times LET_{TH}$$

$$(2.2)$$

where *L* represents the charge collection depth. The value of *L* is technology-dependent and it is in the order of several μ m.

Measurement of Q_{CRIT} can be accomplished by connecting the on-chip sensing circuitry to the target nodes [95], but this is not practical for a complex design. The LET_{TH} can be estimated from irradiation experiments, but only for the whole circuit and not for individual circuit nodes. Hence, the analysis of Q_{CRIT} and LET_{TH} of individual circuit nodes is typically done with device or circuit simulations.

2.4.2 SET Amplitude and Width

The amplitude and width of an SET pulse generated at the output of a logic gate are essential for estimating the probability that such an SET pulse will propagate through the subsequent gates and eventually result in a soft error. In general, the SET pulse width is more commonly used in analysis because the probability that an SET pulse will propagate to a storage element is directly proportional to its width. The SET pulse width is defined as the time interval between the rising and falling edges of the pulse at the level of half of supply voltage. Similarly to Q_{CRIT} and LET_{TH} , the SET pulse width is most commonly analyzed with device or circuit simulations. Direct measurement of SET pulse width under irradiation is possible with the onchip sense amplifiers connected to test points, but this approach is feasible only for simple test circuits [96]. Alternatively, the on-chip digital measurement logic can be used to capture the SET pulse width distribution or the SET count rate for a particular test circuit [97 – 102]. The SET pulse width can be also analyzed with laser exposure, but this requires special preparation of the test chip.

2.4.3 Soft Error Rate (SER)

The Soft Error Rate (SER) denotes the number of soft errors observed in a given time interval, and it can be used to assess the sensitivity of a logic gate, circuit or complete system. Several models for calculation of SER have been reported in literature [19, 20, 103], but the most common is the empirical model proposed by Hazucha and Svensson, which defines the SER of a single node (transistor) as [103],

$$SER = k \times \Phi \times A \times e^{\frac{-Q_{CRIT}}{Q_S}}$$
(2.3)

where k is the technology-independent constant with the value 2.2×10^{-5} , Φ is the flux in particles/(cm²·s), A is the total sensitive area in cm², Q_{CRIT} is the critical charge in fC and Q_{5} is the charge collection efficiency (ratio of collected and generated charge) in fC. The relation (2.3) is known as the nominal or raw SER. The SER is expressed in errors/s or errors/bit/s (for memory and sequential elements). However, for practical reasons, the SER is usually expressed in terms of Failures in Time (FIT), which represents the number of failures per billion working hours. The FIT rate is obtained by multiplying SER with 10^{9} .

As logic gates may have multiple sensitive nodes (transistors), the nominal SER of a logic gate is the sum of the SER values of all sensitive nodes, defined by the relation,

$$SER_{GATE_NOMINAL} = k \times \Phi \times \sum_{i=1}^{M} A(i) \times e^{\frac{-Q_{CRIT}(i)}{Q_S}}$$
(2.4)

where M is the total number of sensitive transistors in a gate. The sensitive area of a transistor is usually approximated with its drain area. Note that the $SER_{GATE_NOMINAL}$ depends on the input logic levels.

The total SER of a combinational circuit is the sum of SER values of all gates in the circuit. Because the SET sensitivity depends on particle LET (which is related to flux), the SER is computed for a predefined range of LET. Thus, for a given LET, the SER of a circuit with *N* logic gates is obtained as [104, 105],

$$SER_{TOTAL} = \sum_{i=1}^{N} SER_{GATE_NOMINAL}(i) \times P_{EM}(i) \times P_{LM}(i) \times P_{TM}(i)$$
(2.5)

where P_{EM} , P_{LM} and P_{TM} represent the masking factors which are equivalent to the probability of electrical, logical and temporal masking, respectively. In literature, the term "derating factors" is also used. The values of P_{EM} , P_{LM} and P_{TM} range from 0 (complete masking) to 1 (no masking). More details on the computation of masking probabilities can be found in [48, 105, 106]. If there are multiple paths from a particular gate to the primary outputs, the total gate SER is calculated as the sum of the contributions of all paths. While the probability of logical masking depends solely on the circuit structure and input logic levels, the electrical and timing masking are directly related to the SET pulse width. For accurate SER computation, it is of utmost important to consider all three masking effects. For example, ignoring electrical masking can result in overestimation of the total SER by more than a factor of 3x [107], while ignoring logical masking can overestimate the SER by 25 times [108], and neglecting timing masking may lead to erroneous estimation of the SER contribution of more than 60 % of gates in a circuit [109].

2.4.4 Cross-Section (σ)

The cross-section σ defines the probability that a particle will hit a sensitive region in a logic gate, circuit or system. It essentially represents the effective area of a gate, circuit or system where a particle hit can cause a soft error, and it is expressed in cm² (or cm²/bit for memory/sequential elements). Thus, lower cross section implies better soft error robustness. It is determined as the ratio between the number of detected errors, *N*_{ERRORS}, and the particle *Fluence*, according to the relation [110, 111],

$$\sigma = \frac{N_{errors}}{Fluence} = \frac{N_{errors}}{\Phi \cdot Time} = \frac{SER}{\Phi}$$
(2.6)

For a given circuit, the cross-section is a function of particle LET, and this dependence is expressed in the form of a four-parameter Weibull curve [110]. The Weibull curve can be obtained from irradiation experiments, and it enables to estimate the LET_{TH} and saturation cross-section for a target circuit.

2.5 Effect of CMOS Technology Scaling on SET Sensitivity

The downscaling of CMOS technologies has brought a significant increase of the SET contribution to the overall SER. This has motivated extensive research to evaluate the contribution of different scaling factors on the SET sensitivity. In this section, a brief review of the scaling trends of SET critical charge (threshold LET), SET pulse width and combinational SER is presented.

2.5.1 Critical Charge (Threshold LET) Scaling

The CMOS technology scaling results in the reduction of critical charge (threshold LET). This is due to the reduction of node capacitance and transistor driving current with the scaling of transistor size and supply voltage. Therefore, a logic gate with a certain driving strength in one technology node will have higher critical charge than an equivalent gate in any lower technology node. As a result of this trend, it has become possible that even the particles with very low energy can cause SETs. For example, while in 250 nm technology an SET could be caused by LET above 15 MeVcm²mg⁻¹, in sub-100 nm technologies a particle with LET of 2 MeVcm²mg⁻¹ is sufficient to cause an SET [78, 80].

Nevertheless, the scaling of critical charge is not uniform with technology scaling. Petersen *et al.* have predicted in 1982 that the critical charge will decrease proportionally to L^2 [112], where *L* is the technology feature size (transistor channel length in µm). However, a recent study of Seifert *et al.* has shown that while in older technologies (above 100 nm) the critical charge reduction was roughly 30 % per generation, in sub-90 nm nodes this reduction is lower (approximately 15 % per generation) due to the adoption of new transistor geometries with reduced sensitive volume [36].

2.5.2 SET Pulse Width Scaling

A comprehensive analysis of the SET pulse width trends with technology scaling has been conducted by Dodd *et al.* [78] and Ferlet-Cavrois *et al.* [113]. Dodd *et al.* have analyzed the 250, 180, 130 and 100 nm bulk and SOI technologies using simulations. On the other hand, Ferlet-Cavrois *et al.* have used the SET current pulses extracted from irradiation of individual transistors to conduct the simulation-based study for

250, 180, 130 and 70 nm bulk and SOI technologies. In both cases the simulations were done for inverter chains. Both works have shown that the SET pulse width dependence on LET does not follow a clear trend with technology scaling. However, both works have confirmed that the SET pulses in bulk technologies are wider than in SOI technologies. Moreover, the works agree that the critical (minimum) SET pulse width for unattenuated propagation decreases as technology scales down.

Besides the aforementioned works, a lot of work was done on experimental characterization of the SET pulse width distribution for different bulk CMOS technologies. The results for technologies from 250 nm to 28 nm are given in Table 2.1 [114 – 118]. The presented results are for nominal supply voltage and room temperature, and inverter chains of different lengths as target circuits. In all cases the irradiation was done with different heavy ions to cover the typical LET range encountered in practice. For the sake of simplicity, here are presented the average and maximum reported SET pulse widths for LET of 60 MeVcm²mg⁻¹. Although the experimental results do not reveal a clear scaling trend, it can be noticed that both maximum and average SET pulse widths remarkably decrease as technology scales below 90 nm. This effect is attributed to the reduction of charge collection volume in scaled technologies. The discrepancies in results for the same technology nodes are caused by the differences in the measurement setups and target circuits. Besides the confirmed decrease of SET pulse width in scaled technologies, an important finding is that the maximum SET pulse width may increase several times when the supply voltage is reduced. For example, Benedetto *et al.* have reported that in 130 nm technology the maximum SET pulse width may be as long as 4.5 ns when the supply voltage is reduced from 1.25 to 1.1 V [114].

Technology node	Reference	Maximum SET width at LET = 60 MeVcm ² mg ⁻¹	Average SET width at LET = 60 MeVcm ² mg ⁻¹	
250 nm	Benedetto et al. [114]	1.5 ns	n/a	
180 nm	Benedetto et al. [114]	1.5 ns	n/a	
120	Benedetto et al. [114]	2.7 ns	n/a	
130 nm	Narasimhan et al. [115]	1.4 ns	650 ps	
90 nm	Narasimhan et al. [115]	1.4 ns	750 ps	
65 nm	Gadlage et al. [116]	200 ps	120 ps	
	Jagannathan <i>et al</i> . [117]	250 ps	175 ps	
28 nm	Jagannathan <i>et al</i> . [118]	230 ps	165 ps	

Table 2.1: Measured SET pulse widths for bulk CMOS technologies

2.5.3 Combinational SER Scaling

For older technologies featuring larger transistors and maximum clock frequencies up to several hundred MHz, the SETs were not a critical issue because it was less probable that they would be induced in large transistors, and even if that happened, the probability of their propagation and latching was very low due to the large propagation delays and long clock periods. However, the studies from 1990s and 2000s have predicted the increasing trend of combinational SER with technology scaling. This was mostly attributed

to the reduction of masking effects in smaller technology nodes, as a consequence of the increase of clock frequency and decrease of supply voltage and logic path length. Nevertheless, there has been a strong disagreement within the research community on the impact of SETs with respect to that of SEUs.

In 1997, Buchner *et al.* suggested that the contribution of combinational logic to the total system SER could eventually exceed that of sequential logic as clock frequencies continue to rise with technology advancement [42]. This prediction was based on the fact that temporal masking decreases linearly with clock frequency, which results in the linear increase of combinational SER with clock frequency. Similarly, based on the results from SPICE simulations, Shivakumar *et al.* [48] predicted in 2002 that the sequential SER will remain almost constant, while the combinational SER will increase by nine orders of magnitude as technology scales from 600 nm (in 1992) to 50 nm (in 2011), and will become a dominant contributor to the total SER for nodes below 50 nm.

However, the aforementioned projections were confronted by a number of later reports. For instance, Mitra *et al.* estimated in 2005 that for a typical microprocessor design, the contribution of combinational logic to the total SER is around 11 %, while the sequential elements (flip-flops and latches) and unprotected SRAMs have the contribution of 49 % and 40 %, respectively [119]. Based on the results from proton and heavy ion irradiation of test chips in 180 nm technology, Gadlage *et al.* reported in 2005 that the SER of a combinational SER is negligible compared to sequential SER, and even decreases slightly from 90 to 65 nm. Similarly, Gill *et al.* [122] reported in 2009 that the combinational SER is less than 30 % of the nominal sequential SER in 32 nm technology. In 2012, Seifert *et al.* demonstrated that the SER of a 10-inverter chain in 22 nm Tri-Gate FinFET technology is around 45 % of the SER of a latch chain at frequency of 3 GHz [35]. Using a commercial SER evaluation tool, Ebrahimi *et al.* demonstrated in 2017 that the combinational SER for OR1200 processor in 45 nm technology increases linearly with frequency, but it is inferior compared to sequential SER or 1 GHz [123].

Along with the above mentioned reports showing that the contribution of SETs to the overall SER is significantly lower compared to that of SEUs, several experimental studies on sub-100 nm technologies have demonstrated that the SER of combinational circuits operating at GHz frequencies may be comparable to or even exceed the SER of sequential circuits. In 2011, Mahatme *et al.* [44] have shown that in 40 nm technology the SER of a flip-flop chain remains constant with the increase of frequency, while the SER of simple combinational circuits increases linearly with frequency, and can account for up to 50 % of the flip-flop SER at 1 GHz, as shown in Figure 2.6. The logical masking is shown to reduce the combinational SER by almost two times. However, by extrapolating the illustrated trend to higher frequencies, the SER of all tested combinational circuits can exceed the SER of a flip-flop chain at clock frequencies beyond 2 GHz [44], as depicted in Figure 2.6. Similar trend was confirmed for 20 and 28 nm technologies [49]. Although these results have been obtained for simple test circuits and hence cannot give a reliable prediction of combinational SER for a complex system, the observed trends are useful as a general reference for future designs in highly-scaled technologies.

The technology scaling trends have also considerable impact on the propagation of SETs through the combinational path. As feature size shrinks below 100 nm, the SET pulse width decreases as shown in Table 2.1. This implies that shorter SET pulses would have more difficulty to propagate through a logic

path. However, the propagation delay of logic gates and the logic path length (number of combinational gates between two flip-flop stages) are also reduced with technology scaling. The propagation delay of logic gates is in the order of dozens of picoseconds for sub-100 nm technologies, while modern digital designs are characterized by short logic paths with no more than 12 logic gates between two flip-flops [44, 48]. As a result, the electrical and logical masking effects are weakened with technology scaling, which facilitates the propagation of SETs and consequently leads to an increase of the combinational SER.

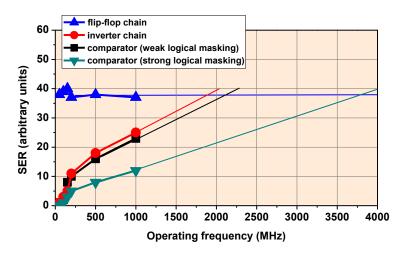


Figure 2.6: Measured SER (thick lines with symbols) and predicted SER (thin lines) as a function of operating frequency, for sequential and combinational logic in 40 nm technology (reproduced from [44])

2.6 Parameters Affecting the SET Sensitivity

Apart from technology scaling effects, the SET sensitivity (combinational SER) can significantly vary for a circuit or system designed in a particular technology. The SET sensitivity of individual logic cells, and thus of the entire system, is determined by a wide range of parameters, which can be classified into five main groups: (i) technology parameters, (ii) design parameters, (iii) operating parameters, (iv) radiation parameters, and (v) other failure mechanisms. In the following, the impact of various parameters on the SET sensitivity is briefly discussed.

2.6.1 Impact of Technology Parameters

The doping concentration and transistor geometry have strong impact on the charge collection efficiency and the shape of SET current pulse. Higher doping concentration results in reduced depletion layer width and funneling length, and consequently in reduced charge collection depth [124]. Hence, technologies with higher doping concentration are more favorable from the perspective of radiation hardness. The transistor geometry defines the active volume where the induced charge can be collected. With the reduction of transistor size in every new generation, the sensitive volume is reduced. For example, the FinFET transistors have smaller charge collection volume compared to standard CMOS transistors, and they are therefore less sensitive to energetic particles. In addition, insertion of isolation layers constraints the silicon regions, thus reducing the collected charge. Such an approach is employed in SOI CMOS technologies, which are inherently more robust to radiation than standard CMOS processes.

2.6.2 Impact of Design Parameters

The standard IC design approach aimed at minimizing the area, delay and power consumption is generally in conflict with the requirements to minimize the SER. It is thus of paramount importance to consider the possible tradeoff between the SER and the design constraints in the early phases of IC design. The design parameters influencing the SET sensitivity of a logic circuit are the size and type of logic gates, load capacitance, capacitance of interconnections and gate placement.

(a) Gate Size

The gate size (driving strength) has a dominant impact on its SET sensitivity. As the transistor's channel length is usually constant for a given technology, the gate size is determined by the channel width. Larger size of sensitive (off-state) transistors means that the sensitive area is larger, and thus the probability that a particle will hit a transistor is higher. On the other side, larger restoring (on-state) transistors have higher driving current, enabling faster dissipation of the particle-induced charge [125]. In addition, larger gates have higher capacitance, which means that more charge has to be induced in order to generate an SET [125]. This implies that, for a fixed load, a larger gate will have higher critical charge and the generated SET pulses will be weaker. However, due to the increase of area, the SER of a larger gate may not be lower than that of smaller gates. Furthermore, large gates have smaller propagation delay (for the same load), and the SETs can more easily propagate through them. Considering carefully the benefits and limitations allows to exploit the gate upsizing for SET mitigation, as will be elaborated in Section 3.4.

(b) Gate Type/Structure

Due to the unique structure of logic gates in terms of the number and arrangement of transistors, the SET sensitivity of different types of logic gates may differ significantly. The sensitive area of logic gates is defined by the number of sensitive transistors. In general, more complex gates would have larger nominal SER. Similarly, logic gates differ in terms of their electrical and logical masking capability due to difference in gate complexity and number of input pins. Therefore, a highly sensitive gate in a circuit can be replaced with a less sensitive logic gate or an alternative logic implementation with lower SET sensitivity. As shown by Limbrick et *al.* [126, 127], replacing a sensitive gate with alternative logic implementations can reduce the generated SET pulse width by approximately 30 %.

(c) Load Size / Fan-out

The sensitivity of a particular gate in terms of SET generation and propagation probability is influenced by the size of load gate(s) and the fan-out (number of load gates). When the load size (or fan-out) increases, the total node capacitance at the output of a target gate also increases, leading to an increase of the critical charge of the target gate's output node. However, the impact of load size on the critical charge is generally weaker compared to the target gate size, as the load size does not affect the driving current in the target gate. In addition, a disadvantage of large load capacitance is that it leads to an increase of SET pulse width. That happens because larger load capacitance needs more time for charging and discharging [128], i.e., more time is required to restore original logic level at the output of target gate. Load upsizing can be also used for SET mitigation, but the aforementioned benefits and limitations need to be taken into account for a given design. More details on the SET mitigation through load upsizing are given in Section 3.4.

(d) Capacitance of Interconnections

The capacitance of interconnections adds to the total node capacitance [125], resulting in higher critical charge of the driving gate's output node. In addition, the capacitance and resistance of interconnections act together as a low-pass RC filter, increasing the propagation delay along the path, and thus enhancing the electrical masking. It has been shown by Bhattacharya *et al.* that short SETs can be attenuated by increasing the interconnection length from x1 to x2, or from x2 to x3, but increasing the length beyond certain limit will not be effective in SET suppression [129].

(e) Gate Placement

The placement of logic gates in the layout may significantly affect the generation of SETs and SEMTs, and thus the overall SER. In general, gates which are adjacent in the circuit netlist may not be physically close in the layout. Ebrahimi *et al.* [82] and Huang *et al.* [130] have shown that by rearranging the logic cells in the layout in order to increase the spacing between critical cells and thus reduce the probability of SEMTs, the total SER can be reduced by at least 20 %, with negligible area overhead. Likewise, by placing the electrically connected logic gates close to each other, the generated SETs can be attenuated due to pulse quenching. As demonstrated by Pagliarini *et al.* [131] and Yankang *et al.* [132], an improvement of SER by 10 - 16 % can be achieved if cell placement is done considering the pulse quenching phenomenon.

2.6.3 Impact of Operating Parameters

The operating parameters may vary during the runtime as a consequence of the variation of workload and operating/environmental conditions. This results in the real-time variation of the SET sensitivity and the overall system SER. The operating parameters with strongest impact on the SET sensitivity are: input logic levels, supply voltage, clock frequency and temperature.

(a) Input Logic Levels

The logic levels at the inputs of combinational gates determine the on/off state of transistors within the gate, and thereby directly affect the SET generation process. Both the critical charge and the SET pulse width may vary as the input levels are changed, resulting in the real-time SER variation. Rezaei *et al.* have shown that the computed SER for ISCAS89 benchmark circuits may differ by 38 % when the impact of input levels is taken into account compared to the case when input levels are ignored [133]. The input levels also determine the equivalent resistance of the gate, and therefore affect the gate's propagation delay. This means that the width of an SET pulse propagating through a logic gate will vary depending on the input pin at which it arrives.

(b) Supply Voltage

To supply voltage may vary significantly across an IC. Complex ICs usually have multiple power domains, where each domain has its own supply voltage. To reduce the power consumption in a complex IC, the dynamic voltage and frequency scaling (DVFS) approach is usually applied. In addition, small voltage fluctuations (tens of mV) may occur during normal system operation, due to the non-zero resistance and inductance of supply wires. As the supply voltage determines the transistors' driving current, decreasing the supply voltage reduces the gates' capability to dissipate the induced charge, resulting in lower critical

charge (less charge is required to cause an SET at lower supply voltage). The induced SETs will therefore be longer at lower supply voltage. The dependence between critical charge and supply voltage is close to linear, but due to the exponential relationship between critical charge and SER, a small variation in supply voltage may result in significant SER changes. For example, Dixit and Wood have shown that the reduction of supply voltage by 0. 1 V increases the cell-level SER by 3 times [34]. On the other hand, lowering the supply voltage increases the propagation delay of logic gates, allowing better SET filtering. Therefore, for accurate SER evaluation it is mandatory to take into account the impact of supply voltage on both SET generation and propagation. As demonstrated by Kiamehr *et al.*, neglecting the impact of supply voltage variability may lead to an error in SER computation greater than 150 % [134].

(c) Clock Frequency

The clock frequency affects the combinational SER through its impact on the latching probability, but it has no effect on the SET generation and propagation. Due to the linear dependence between the combinational SER and clock frequency, the frequency reduction is an effective approach for lowering both the SER and the dynamic power consumption, without area overhead. However, the cost of frequency scaling is the reduced system performance.

(d) Temperature

Depending on the application, the operating temperature of an IC may vary over a wide range. For example, a typical operating temperature range for the space-qualified ICs is from -55 to 125 °C. The temperature increase leads to a decrease of critical charge, and an increase of SET pulse width. This is attributed to the reduction of carrier mobility at elevated temperatures, which results in a decrease of the transistors' driving strength, and consequently in the weakening of the circuit's ability to dissipate the induced charge. Bagatin *et al.* have shown that the critical charge may decrease by around 12 % as temperature increases from 20 to 80 °C [135], while Gadlage *et al.* have shown that the SET pulse width increases by more than 30 % due to temperature rise from 25 to 100 °C in 90 nm technology [116]. Hsueh *et al.* have calculated that the SER of ISCAS85 benchmark circuits in 45 nm technology increases by 145 % from 25 to 100 °C [136]. However, as shown by Sootkaneung *et al.* [137], for newer technologies (14 nm FinFET) the temperature effect is reversed, i.e., increase in temperature leads to an increase in critical charge.

2.6.4 Impact of Irradiation Parameters

As elaborated in previous discussion, the radiation parameters that have strongest impact on combinational SER are particle flux, LET, angle of incidence and strike location. The increase of particle flux leads to a linear increase of SER according to the relation (2.3), but it has no direct influence on the critical charge or SET pulse width. On the other side, the particle LET, angle of incidence and strike location determine the SET generation process, i.e., the SET current pulse and the corresponding SET voltage pulse. The amount of deposited charge is linearly related to LET, according to the relation (2.1). Both high LET and angular strikes are particularly critical, as they strongly contribute to the generation of longer SETs as well as SEMTs, thus increasing the SER. The strike location and angle of incidence are totally random and cannot be predicted in advance. On the other hand, the LET and flux variations can be measured in real-time, enabling to dynamically monitor the SER variations.

2.6.5 Impact of Other Failure Mechanisms

The failure mechanisms inherent in modern CMOS technologies may affect simultaneously the SER of an IC. For example, the process variations, manufacturing defects and aging are shown to have significant impact on the SER. Due to process variations, the transistor's channel width and length may deviate from the predefined values, resulting in the change of critical charge by at least 10 % [138]. We have shown with circuit simulations that the intra- and inter-gate resistive open and short defects may cause the decrease of critical charge of combinational logic up to 80 % [MA12]. As a result of aging, caused mainly by the Bias Temperature Instability (BTI) and Hot Carrier Injection (HCI), the absolute value of transistors' threshold voltage increases over time, leading to a gradual degradation of transistors' driving current and reduction of critical charge. Rossi *et al.* have estimated that the critical charge of basic combinational gates (INV, NAND and NOR) may decrease 15 - 22 % after ten years of in-field operation, which accounts for more than 17 % increase of the SER of ITC99 benchmark circuits [139].

2.6.6 Relative and Combined Impact of Multiple Parameters

Previous discussion has shown that the SET sensitivity (SER) of combinational logic is a complex function of a multitude of design, operating, technology and irradiation parameters. The mechanisms underlying the SET response of CMOS combinational logic are well understood and documented in literature. However, the main challenge is related to accurate and efficient characterization and modeling of these effects at different abstraction levels of the design process.

Although multiple parameters may have qualitatively similar effect on SER, i.e., cause either linear or exponential increase/decrease of SER, their quantitative contribution may differ significantly. For instance, the critical charge increases proportionally to the size of target and load gates, but the target gate size has stronger quantitative impact. Furthermore, certain parameters (e.g., gate size) may have opposing effects on SET generation and SET propagation. Another important aspect is the combined impact of multiple parameters, which might produce significantly different results than when considering the parameters separately. The combined impact of multiple parameters can be also exploited for reducing the overall SER. For example, the increase in SER due to increase in particle flux can be compensated to a certain extent by increasing the supply voltage and/or decreasing the clock frequency.

With respect to the aforementioned issues, the main goal of the characterization of SET effects is to evaluate both quantitative and qualitative contribution of relevant parameters, as well as their combined impact. Based on characterization results, the predictive models for SET sensitivity in terms of design, operating and irradiation parameters, can be established for a given technology. This can ease the analysis of SET effects in a complex design, enabling a more time-efficient design of rad-hard ICs.

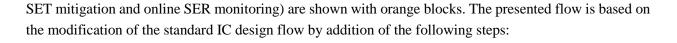
Chapter 3

Related Work

This chapter reviews the state-of-the-art with respect to the three main topics addressed in this thesis: (i) characterization and modeling of SET effects in standard combinational cells, (ii) gate-level SET mitigation, and (iii) particle detection for the online SER monitoring, as a support for the self-adaptive fault tolerance. The chapter is divided into six sections. In Section 3.1, a multi-level rad-hard design flow is introduced. Section 3.2 discusses the SET characterization methodologies with the focus on the simulation-based characterization of SET effects in standard digital cell libraries. Section 3.3 reviews the predictive models for SET effects - SET current models, SET critical charge models, SET pulse width models and SET propagation models. Section 3.4 discusses the benefits and limitations of existing gate-level techniques for mitigation of SET effects in combinational circuits. Section 3.5 analyzes the main advantages and disadvantages of existing solutions for the online particle detection from the perspective of requirements in the self-adaptive fault-tolerant applications. Finally, in Section 3.6, the open issues that will be addressed in this work are summarized.

3.1 A Multilevel Radiation-Hardening-By-Design Flow

The radiation-hardening-by-design (RHBD) process involves two main phases: (i) *characterization and modeling of soft error effects*, and (ii) *application of soft error mitigation measures*. In addition, if the self-adaptive (dynamic) soft error mitigation is required, the *online soft error monitoring* has to be employed. The characterization and mitigation are performed at multiple abstraction levels, from device to system level. This process involves a trade-off between the required SER defined by the application requirements and the design constraints related to the chip area, performance and power consumption. Although the use of a custom-designed rad-hard library usually provides the best results, this approach is too costly. Thus, a widely accepted methodology is based on the use of non-rad-hard standard libraries which can provide acceptable performance with appropriate design measures. The characterization and mitigation procedures are conducted in an iterative manner, until the minimum (or required) SER of a target design flow supporting the soft-error-aware design concept illustrated in Figure 1.2 can be represented as in Figure 3.1 [140]. The three main aspects addressed in this work (characterization of SET effects in standard cells, gate-level



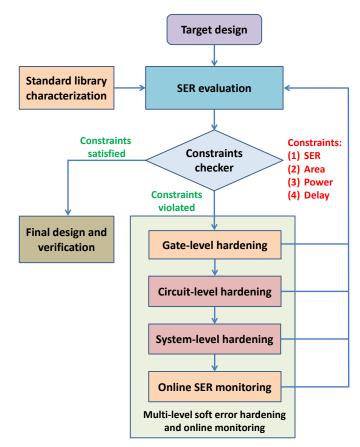


Figure 3.1: A multi-level rad-hard design flow for standard-cell-based IC designs

- *Standard library characterization*: The soft error sensitivity of each standard cell in a given library is characterized with electrical simulations for a range of design, operating and irradiation parameters. The characterization results are stored in respective LUTs. To ease the application of LUT database in the SER analysis of a target design, the analytical models for soft error generation and propagation are derived from the simulation results. Although the library characterization is generally done once, it may need to be repeated for custom-designed rad-hard cells (e.g. rad-hard flip-flops, SET filters, etc.) which may be subsequently added to the library.
- *SER evaluation*: The SER of a target design is evaluated employing the characterization LUT database and respective SER models. Depending on the information obtained from the library characterization, the SER of a target design can be computed only with analytical evaluation, with limited fault-injection simulations, or with combination of analytical methods and simulations. In any case, for accurate SER calculation, the analysis should consider the soft error generation effects as well as the impact of all relevant soft error propagation effects.
- *Multi-level soft error mitigation and online monitoring*: For efficient soft error mitigation, multiple design techniques have to be implemented to reduce the SER of the most sensitive elements in the target

design. To achieve a trade-off between the desired SER and the area, power and performance constraints, the mitigation measure are applied at gate, circuit and system levels, combining static and dynamic solutions. To allow for autonomous triggering of dynamic fault-tolerant mechanisms, the detectors of energetic particles causing the soft errors have to be integrated in the design.

• *Constraints checking:* Since the applied hardening measures are effective as long as they do not violate the predefined design constraints, the area, delay and power have to be recalculated after applying the soft error mitigation measures. When the required SER is achieved, the remaining design and verify-cation phases from the standard IC design flow are conducted.

3.2 SET Characterization in Combinational Logic

The ultimate objective of the SET characterization process is to identify the combinational gates in a given circuit with largest contribution to the total SER. This is accomplished by analyzing the SET generation and propagation effects for each gate. The characterization results serve as a guideline for the circuit designers in selection of the most appropriate hardening methods. Basically, the SET characterization investigates the dependence of the SET sensitivity metrics in terms of a range of design, operating and irradiation parameters, for a given technology. This is generally a complex task because the SET pulses can have various shapes, amplitudes and widths, while any target combinational design contains a wide variety of standard cells. Thus, there is a strong need for optimized SET characterization methodology that can save both time and resources.

3.2.1 Simulation-Based and Analytical Characterization Methodologies

Two methodologies for characterization of SET effects in the early design phases are: (ii) *simulation-based characterization* [141 – 146], and (ii) *analytical characterization* [147 – 159]. Note that both approaches are also applicable for the characterization of SEUs.

The simulation-based approach allows to analyze the SET effects at multiple abstraction levels, thus providing a detailed insight into the sensitivity of each element. Figure 3.2 illustrates the hierarchy of simulation-based SET characterization with four main abstraction levels: particle-matter interaction level, device level, circuit level and system level. At each level, dedicated models of radiation-induced effects and simulation tools are employed. The results from each level are utilized as inputs for the subsequent higher abstraction levels. Performing the SET simulations at any of the aforementioned abstraction levels enables to capture the SET characteristics which cannot be efficiently analyzed at other levels. However, at the same time, each abstraction level brings some limitations due to which the analysis at one level is not sufficient for accurate SER evaluation.

At the particle-matter interaction level, the deposited charge, particle's LET and track length in silicon are obtained using Monte Carlo-based tools such as SRIM/TRIM [160], PHITS [161], or MRED [162]. These simulations are quite fast, lasting from seconds to minutes. With this information, the device-level simulations are performed to obtain the charge collection profiles (radiation-induced current pulse shape) in a single transistor, as a function of technology and irradiation parameters. The device simulations can be also used to analyze the SET voltage pulse in a single transistor. For this purpose, the Technology Computer

Aided Design (TCAD) tools such as Synopsys Sentaurus [163] or Silvaco Victory [164], are used. Although TCAD simulations provide accurate analysis of the impact of technology parameters (doping profile and transistor geometry) and radiation parameters (LET, strike location and angle of incidence), they are very time-consuming. For example, one simulation run for a single transistor may take several hours. The SET current pulses from TCAD simulations are applied in the electrical (circuit) simulations to assess the impact of induced SETs on the electrical response of a logic gate or a circuit. For this purpose, dedicate current sources are connected to the target nodes. This analysis is performed with SPICE (Simulation Program with Integrated Circuits Emphasis)-compatible simulators such as Cadence Spectre [165]. By coupling SPICE and TCAD simulations in the form of so-called mixed-mode simulations, the effects in one transistor within a given circuit can be analyzed. The SET propagation through a complex digital design is evaluated with logic simulations at the Register-Transfer Level (RTL) or system level, using the hardware description language (HDL)-based tools such as ModelSim [166], or customized fault injection tools such as Cadence Incisive Fault Safety Simulator (IFSS) [167]. The SETs are modeled at RTL level as digital pulses with predefined duration, which is obtained from electrical simulations. Along with the aforementioned standard commercial design tools, various customized tools can be utilized for the analysis of radiation effects and SER computation. Several well-known examples are TFIT and SOCFIT [168], CRÈME96 [169], Musca-SEP [170], and MC-Oracle [171]. The use of these tools for SER analysis requires the information on the radiation conditions, target circuit design, and target technology.

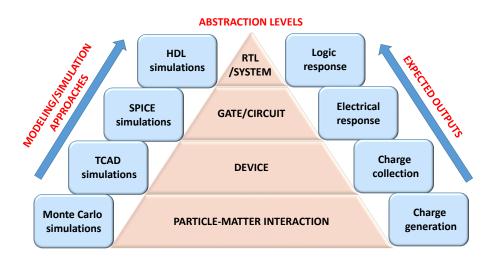


Figure 3.2: Hierarchy of multi-level simulation-based SET characterization

Performing the multi-level SET simulations for every design would be computationally-intensive. In addition, such an approach is even not practical because the particle-matter interaction and device-level analysis can be conducted off-line, for a given technology and a limited number of selected devices. These results can then be applied to evaluate a given design through the circuit and RTL simulations. Generally, the circuit and RTL simulations are performed by exhaustive fault injection campaigns, i.e., electrical or logical faults are injected in all circuit nodes, and for all possible combinations of input vectors. The ratio between the number of injected faults and the number of faults observed at the primary outputs represents a measure of the soft error robustness. However, the SPICE simulations are applicable only to small circuits (tens of logic gates) because the simulation runtime increases exponentially with the number of gates. The

electrical simulations can be optimized using the method of equivalent gates [146], but this approach reduces the accuracy and it is still very time-consuming even for moderate-size circuits with thousands of gates. The RTL fault injection simulations may be orders of magnitude faster than electrical simulations. Nevertheless, performing the RTL simulations for all possible input vector combinations and all gates in the target design becomes intractable for designs with millions of gates and tens of inputs. It is possible to reduce the number of RTL fault injection simulations by using a subset of input vectors or performing the simulations only for a subset of circuit nodes. Although this may significantly reduce the simulation runtime, the accuracy of SER evaluation is also reduced.

In order to alleviate the runtime issues of simulation-based approaches, various analytical methods have been introduced. These methods employ mathematical or algorithmic models at RTL level, and the SER is estimated through statistical analysis of the design. The most common approaches are based on: Binary Decision Diagrams (BDD) / Algebraic Decision Diagrams (ADD) [147, 148], (ii) Boolean satisfiability theory [149 – 151], and (iii) Error Propagation Probability (EPP) [152 – 155]. The analytical approaches may be orders of magnitude faster than the simulation-based fault injections, and they are in most cases very accurate in evaluation of logical masking probability. However, these methods require extensive processing, and they neglect physical and electrical SET characteristics such as charge collection profiles and SET current and voltage parameters. As a result, the overall accuracy of analytical SER evaluation methods is usually lower compared to simulation-based analysis. Several methods have been recently proposed to optimize the analytical SER evaluation. The analysis based on structural properties of the circuit [156, 157] and the method of circuit partitioning [158] have been used to reduce the analysis runtime. Recently, the Answer SET Programming (ASP) approach, employing highly optimized ASP solvers that do not require complex pre-processing, has been proposed [159].

3.2.2 A Two-Phase Combinational SER Evaluation

With the growing complexity of digital designs, the scalability issues have become a limiting factor for both analytical and simulation-based SER evaluation approaches. Individual digital blocks within a complex design may have from thousands to hundreds of thousands of standard cells. In addition, the number of input vector combinations increases exponentially with the number of inputs. Extensive work has been done in the past two decades to provide fast, accurate and efficient SER characterization methods by reducing the number of simulations and the amount of data required for analysis. In order to leverage the benefits of simulation-based and analytical approaches on one hand, and alleviate their intrinsic limitations on the other hand, numerous works have adopted a methodology which combines these two approaches into a unified evaluation framework composed of two phases:

- (i) Characterization of SET effects in a standard cell library (performed with simulations)
- (ii) SER evaluation of a target design (performed analytically)

A general flow illustrating the main steps during the characterization of SET effects in a standard library and the SER evaluation of a target design is illustrated in Figure 3.3. Note that these two phases are part of the general multi-level rad-hard design flow illustrated in Figure 3.1. The standard library characterization is performed only once, while the SER evaluation is performed for each new design mapped to the standard cells. The usual approach is to characterize first the standard library with simulations, whereas the SER of

a target circuit is determined by employing the library characterization results and the analytical methods. The rationale for performing the library characterization is the fact that every digital circuit is composed of multiple gates of the same type, and the SET sensitivity of each gate is strongly dependent on the design parameters such as gate size (driving strength), load size (fan-out) and gate position in the circuit. Thus, it is not practical to conduct electrical or logic fault injection for every circuit node if the SET sensitivity of standard logic gates can be pre-characterized under different design and operating settings.

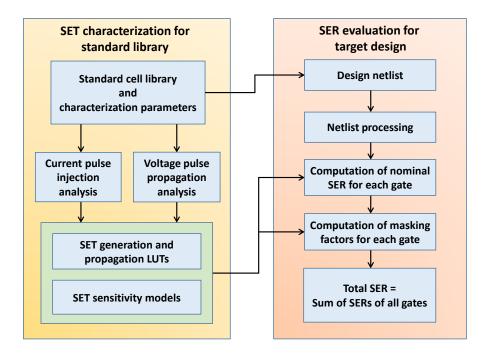


Figure 3.3: A general two-phase combinational SER evaluation flow

During the standard library characterization, the SET generation and propagation for each gate is evaluated, and the SET characterization database and/or the SET sensitivity models are constructed. The SET database and SET sensitivity models obtained from characterization are applied for evaluation of the SER of any design composed of pre-characterized cells. The SER evaluation is performed with custom-designed automated tools that employ analytical methods for static circuit analysis. This phase starts with the design netlist processing, which involves parsing of netlist to identify the composition of the circuit, and then based on this the design is analyzed with an appropriate analytical model. The nominal SER and masking factors are computed for each gate based on the characterization database, and the sum of all SERs gives the total SER according to the relation (2.5).

Although significant results have been achieved so far, there is still no an optimal and standardized SET characterization methodology that is compatible with the standard industrial design flows. The existing methodologies for standard library characterization and analytical SER evaluation still suffer from a number of inherent limitations in terms of accuracy and runtime. As this work addresses the standard library characterization, as the main prerequisite for efficient SER evaluation, in the following discussion various approaches for characterization of SET effects in standard libraries are presented.

3.2.3 SET Characterization of Standard Cell Library

The characterization of SET effects in standard cells is performed with electrical (SPICE-like) simulations, and to certain extent also with TCAD simulations. The aim is to capture the electrical aspects of the SET generation and propagation effects for individual standard cells, allowing to compute the nominal SER, electrical masking and PIPB for each gate. Based on characterization results, the electrical and timing masking factors for each gate in a given circuit can be determined. The characterization procedure involves the analysis of SET sensitivity metrics in terms of design, operating, and irradiation parameters described in Section 2.6. Unlike the logical masking, the electrical and timing masking effects depend on a wide range of parameters. Therefore, the electrical and timing masking calculations may be orders of magnitude less accurate than logical masking if the key contributing parameters are neglected [172]. The standard library characterization consists of two main tasks:

- *SET generation analysis* Evaluation of critical charge and SET pulse width/amplitude at the output of a logic gate in terms of gate size, load size (load capacitance), supply voltage, temperature, input logic levels, LET, etc. This allows to determine the nominal SER for each gate.
- *SET propagation analysis* Evaluation of the change of SET pulse amplitude and/or width as it propagates through a logic gate, in terms of the contributing parameters. This allows to estimate the electrical and timing masking factors.

In the SET generation analysis, the current injection approach is applied on the transistor level of standard cells. A suitable current source is employed as a model of the SET current pulse. The parameters of the current model are obtained from TCAD simulations or experimental measurements. An overview of the most common SET current models is given in Section 3.3.1. By injecting the current pulse in sensitive nodes of the gate (drain terminals of transistors), the amplitude and width of the SET pulse generated at the output of the gate, and the critical charge for all sensitive nodes in the gate, can be obtained for different design, operating and irradiation settings.

In the SET propagation analysis, a voltage pulse representing the generated SET pulse is fed to one input of the target gate, while other inputs are set to logic values which enable the signal propagation. This analysis is repeated for all input pins. The rectangular or trapezoidal voltage pulses are typically used for simulation of SET propagation effects. The variation of the amplitude, width and transition times of the output SET pulse is analyzed in terms of the parameters of input SET pulse and other relevant design and operating settings. The parameters of the input pulse are selected based on the SET generation analysis. As a result of propagation analysis, the electrical masking and PIPB effects for each gate can be captured, enabling to compute the electrical masking and pulse broadening for a given logic path.

For each standard cell, two sets of two-dimensional (2D) LUTs, the SET generation LUTs and the SET propagation LUTs, are constructed to store the simulation results. Each LUT depicts the variation of a particular SET metric in terms of two contributing parameters, for the nominal values of other contributing parameters. For example, one LUT can store the critical charge values for all inputs and driving strengths of a target gate. In general, the number of LUTs depends on the number of characterized standard cells, SET metrics and contributing parameters. Once the LUTs for all gates are established, the linear interpolation may be applied to obtain the results for values which are not in the LUTs.

Extensive work has been done in relation to the characterization of SET effects in standard cell libraries, and various characterization methodologies have been reported [90, 104, 108, 136, 173 – 186]. Although all reported methods employ the previously discussed basic approach, there are differences in terms of the used SET current models, number of analyzed parameters and structure of the characterization LUTs. The most important features of the reported methodologies are summarized in Table 3.1. All methodologies provide a high accuracy with respect to SPICE, for the conditions considered in simulations. However, each of them has at least one of the following drawbacks:

- In most cases the bias-independent SET current models such as the double-exponential current model [187 189] or single-exponential current model [190] are used for SET generation simulations. These models are inaccurate for the SET pulse width characterization, as will be explained in the following section.
- Some essential parameters affecting the SET response are neglected during the characterization in
 order to simplify the analysis. For example, many approaches do not consider the supply voltage
 or temperature variations, and most approaches do not take into account the impact of timing parameters of the SET current pulse or the capacitance of interconnections. As elaborated in Section
 2.6, neglecting these parameters leads to high errors in SER computation.
- Most characterization methodologies perform the simulations for all gates and all combinations of contributing parameters. Although the library characterization is done once, this may still be very time consuming as the standard libraries may have hundreds or even thousands of standard cells. As demonstrated in [183], the characterization of 10 standard combinational cells requires 570k simulations for SET generation and 6M simulations for SET propagation.
- A large number of LUTs resulting from the characterization process often make the subsequent SER evaluation more complex because the LUTs have to be accessed and read continuously during the evaluation of a target design. In addition, the LUTs do not show explicitly the relationship between the SET sensitivity metrics and the contributing parameters, which imposes the need for additional processing (e.g., fitting has to be applied for values which are not in LUTs).

The aforementioned limitations of existing methodologies impose the need for exploring new solutions for optimized characterization of SET effects in standard combinational cells. An approach to reduce the number of simulations and the amount of characterization data is by employing analytical models for predicting the SET sensitivity. One class of such models are the physics-based SET sensitivity models. These models are derived analytically, considering the details of the physical mechanisms and technology parameters. However, the main limitations of the physics-based models are: (i) details of the physical mechanisms and technology are often not available to the designer, and therefore the adoption of the model to a new technology may be challenging, (ii) physics-based models incorporate many parameters which are not directly involved in the rad-hard design process and therefore may not be useful in every application. An alternative approach is based on derivation of SET sensitivity models by fitting the characterization results stored in LUTs. These models are then incorporated in the subsequent SER evaluation of a target design. A variety of models have been proposed for SET critical charge, SET pulse width and SET propagation. However, the aforementioned limitations of the LUT-based characterization are reflected in the accuracy of the fitting models. Most existing models consider a limited set of parameters, which limits

their ability to predict the SET effects under different realistic scenarios. A more detailed overview of the SET sensitivity models is given in Section 3.3.

In addition to the aforementioned shortcomings, the characterization methods presented in Table 3.1 have an important common drawback: **none of them addresses the characterization of gate-level SET mitigation techniques**. As a result, additional characterization has to be performed to choose the optimal gate-level hardening solutions for a target design, which may be very time-consuming since the SER analysis and the hardening measures are applied iteratively in the rad-hard design flow, as illustrated in Figure 3.1. A detailed discussion on the gate-level SET mitigation techniques is given in Section 3.4.

Therefore, for accurate and efficient SER characterization and subsequent application of SET mitigation solutions, **it is crucial to address synergistically the characterization of the standard cell library and the respective gate-level mitigation solutions.** To ensure that the characterization results can be applied to different SER evaluation approaches, the characterization process should: (i) consider all parameters relevant in the IC design, (ii) be optimized and time-efficient irrespective of the target library size, and (iii) provide a detailed SET database and accurate SET sensitivity models.

Reference	ference Short description of characterization approach	
Gill et al.,	Using a single-exponential current source, the width of SET pulse generated at the	
2005 [173]	output of each cell in terms of particle energy and load capacitance is analyzed.	
	Applying a trapezoidal voltage pulse to every input of a cell, the output pulse width	
	in terms of the input pulse width and capacitive load is analyzed.	
Zhang et al,	The current injection with a single-exponential current source is applied. The SET	
2006 [108]	pulse width and amplitude at the output of each cell are analyzed in terms of input	
	logic levels, injected charge and load capacitance. For SET propagation analysis, a	
	trapezoidal pulse is propagated through each cell, and the output pulse width and	
	amplitude are found as a function of input pulse width and amplitude.	
Rajaraman et	The current pulses extracted from device simulations are injected in each cell and the	
al., 2006 [174]	corresponding voltage pulse at the cell's output is analyzed in terms of capacitive	
	load. The output voltage pulse is characterized in terms of the width, amplitude and	
	rise and fall time constants. In addition, the delay of each cell is characterized for	
	propagation analysis. Based on characterization results, a mathematical model for	
	electrical masking of a single gate is derived.	
Rao et al.,	A single-exponential current source is used. For nominal supply voltage, the SET	
2007 [175]	pulse width generated at the output of each cell is characterized in terms of injected	
	charge, gate size, load size and input logic levels. Based on characterization results,	
	a model of SET pulse is derived in the form of Weibull function.	
Zhao et al.,	The SET generation is characterized with a double-exponential current source, and a	
2007 [176]	characterization matrix is formed to represent the probability that an SET pulse with	
	certain amplitude and width will be generated at the output of a target gate. The SET	
	propagation is characterized by constructing a matrix which stores the SET amplitude	
	and width at the output of a gate as a function of input SET pulse width and amplitude,	
	load capacitance and input pulse polarity.	

Table 3.1: Summary of methodologies for SET characterization of standard cell libraries

Ramakrishnan et	A double-exponential current source is used to characterize the SET generation in	
al., 2008 [177]	typical logical blocks composed of standard cells. The output database represents a	
un, 2000 [177]	set of voltage pulses at the outputs of targets block in terms of a set of current pulses	
	injected in different nodes within the block. For propagation analysis, the amplitude	
	and width of SET pulses at the outputs of target blocks are characterized in terms of	
	the amplitude and width of input pulses.	
Kuo et al.,	The amplitude and width of generated and propagated SET are extracted from Monte	
2010 [178]	Carlo SPICE simulations with a double-exponential current source. For each cell, the	
	induced charge, loading capacitance, SET pulse polarity and process variation are	
	considered. The mean and variance for generated and propagated SET pulse width	
	distribution is obtained.	
Pontes et al.,	The current injection with the double-exponential current model is applied. The	
2012 [179]	critical charge and output SET pulse width and amplitude are analyzed for all input	
	levels. The Liberty standard is adopted for storing the characterization results. This	
	approach requires to modify the standard cells by insertion of an additional pin for	
	triggering the SETs.	
Kiamehr et al.,	SET propagation through standard cells is characterized in terms of supply voltage	
2013 [134]	and amplitude, width and rise/fall slopes of input SET pulse. A trapezoidal voltage	
	pulse is used to model the input SET pulse. Analysis is done with SPICE simulations	
	and all results are stored in LUTs.	
Hamad et al.,	Using SPICE simulations, the SET propagation through standard cells is analyzed as	
2014 [90]	a function of input levels, SET polarity and fan-out. The magnitude of the pulse	
_01.[20]	broadening/narrowing is stored in LUTs, and an analytical model for the propagation-	
	induced SET pulse width variation is proposed.	
Hsueh et al.,	A double-exponential current source with fixed timing parameters was utilized to	
2014 [136]	characterize the temperature dependence of the generated and propagated SET pulse	
2014 [150]	width at the output of standard logic cells. Characterization was done for different	
	values of injected current (charge) and load capacitances.	
Evans et al.,	A simulation tool TFIT, which combines TCAD and SPICE simulations, is used to	
	characterize the FIT rate of standard cells. For each cell, the FIT rate as a function of	
2014 [104]		
	SET pulse width is obtained. Besides, a number of digital blocks are characterized in	
	terms of their nominal FIT rate and derating factors. This approach considers the	
	layout of standard cells as well as the real radiation environment.	
Assis et al.,	Using a charge collection model calibrated with TCAD simulations, the current	
2015 [180]	injection is performed through SPICE simulations to obtain the SET pulse width at	
	the output of standard cells. Simulations are done only for inverter, and the response	
	for other gates is obtained by mapping each gate to equivalent inverters. The model	
	for generated SET pulse width, considering the pulse quenching effect, is derived.	
Farahani et al.,	A double-exponential current source is used to characterize the SET generation, while	
2015 [181]	a trapezoidal voltage pulse is used for characterization of SET propagation. The	
	amplitude and width of generated and propagated SET pulse are analyzed for each	
	cell. The approach considers the impact of transistor channel width and length,	
	threshold voltage, load capacitance, input logic levels, supply voltage, temperature,	
	process variations and aging. For propagation analysis, the transition times of the	
	input trapezoidal pulse are also considered.	
	amplitude and width of generated and propagated SET pulse are analyzed for each cell. The approach considers the impact of transistor channel width and length, threshold voltage, load capacitance, input logic levels, supply voltage, temperature, process variations and aging. For propagation analysis, the transition times of the	

Diana at al	Comment injection is negligeneral in all consistive modes of standard with the		
Riera et al.,	Current injection is performed in all sensitive nodes of standard cells, using the		
2016 [182]	double-exponential current source. Critical charge is determined for each node, all		
	input logic levels, and different values of supply voltage, temperature and timing		
	parameters of the current source. With these results, the nominal SER for each gate		
	is computed as an average of the SER values for all input levels. The SET propagation		
	is not characterized.		
Sheng et al.,	Piecewise linear approximation of single-exponential current source is used. For SET		
2016 [183]	generation, the SET pulse width and amplitude at cell output are analyzed in terms of		
	injected charge, load capacitance and input levels. For SET propagation, the SET		
	pulse width and amplitude at the cell output are analyzed in terms of amplitude and		
	width of input pulse and load capacitance.		
Du et al.,	A grid-based approach, which considers the cell layout, is used to characterize the		
2016 [184]	standard cells. The SET pulse width for different strike locations is captured from		
	TCAD simulations and stored in LUTs. The linear interpolation is used to determine		
	the SET pulse widths for the strike locations that are not considered in analysis. The		
	SET pulses are injected in a given circuit to assess the SET propagation effects.		
Li et al.,	Current injection with double-exponential current source is applied to characterize		
2017 [185]	the SET generation and propagation for each cell. For SET generation, the SET		
	voltage pulses for different current source settings are recorded, and for each gate		
	size and input combination, one LUT is constructed to store the SET pulse width		
	different deposited charge and load capacitance. For SET propagation, and for each		
	gate and input combination, one LUT is formed to express the output SET pulse width		
	in terms of input SET pulse width and load capacitance.		
Aguiar et al.,	A commercial tool MC-ORACLE is used to extract the SET current database for each		
2019 [186]	cell, taking into account the cell layout. The current database is then applied in SPICE		
	simulations to characterize the cross-section for each gate in terms of driving strength,		
	input levels and supply voltage.		

3.3 SET Models

This section reviews the key features of existing SET models. The SET models are used to represent in analytical form the SET generation and propagation effects, thus allowing to predict the response under real irradiation. Using the models simplifies the SET characterization process and enables faster estimation of the SER of a given design. The SET models can be categorized as:

- **SET current models** represent the shape of the current pulse induced in a device by an incident energetic particle.
- **SET critical charge models** represent the critical charge as a function of design, operating, technology and irradiation parameters.
- **SET pulse width models** represent the shape, width or amplitude of the SET voltage pulse at the output of a logic gate as a function of design, operating, technology and irradiation parameters.
- **SET propagation models** represent the change of the amplitude and/or width of the SET voltage pulse as it propagates through the subsequent logic gates, as a function of design, operating, technology and irradiation parameters.

3.3.1 SET Current Models

The SET current models are used for simulation of the SET generation process at the circuit level. They are implemented in circuit simulations as SPICE/Spectre or Verilog-A current sources. Two modeling concepts for the SET-induced current are (Figure 3.4):

- (i) Macro-model: a current source is connected between target node and ground.
- (ii) Micro-model: a current source is integrated in the transistor.

In general, the macro-modeling concept is more common because it is easier for implementation in circuit simulators. On the other hand, the micro-model should be integrated in the target transistor, which requires the modification of existing transistor models. In principle, the same current model may be used for simulating the particle hits in both PMOS and NMOS transistors, and the only difference will be in the direction of the current flow.

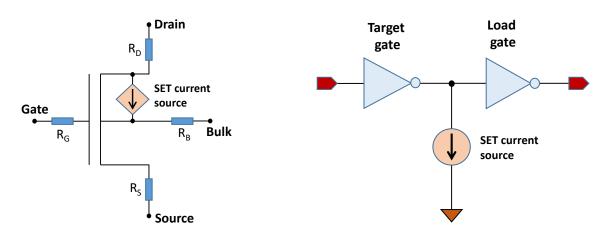


Figure 3.4: SET current models: micro-model (left) and macro-model (right)

Numerous models for circuit-level simulation of SET-induced current have been proposed, and they can be classified into five major types:

- (1) SET current models based on single bias-independent current source.
- (2) SET current models based on bias-dependent current source.
- (3) SET current models based on two bias-independent current sources.
- (4) SET current models based on piecewise interpolation.
- (5) SET current models based on look-up table.

In the following, the key features of each SET current model type are briefly described. A more detailed comparative analysis can be found in [MA11].

3.3.1.1 Current Models Based on Bias-Independent Current Source

The double-exponential current model is the most widely used SET current model. It represents the SET current pulse shape with fast rise and slow decay, as illustrated in Figure 2.3 (a) in Chapter 2. The analytical expression has been formulated by Messenger [187], as follows,

$$I_{SET}(t) = \frac{Q_{COLL}}{\tau_{fall} - \tau_{rise}} \left(e^{\frac{-t}{\tau_{fall}}} - e^{\frac{-t}{\tau_{rise}}} \right)$$
(3.1)

In relation (3.1), Q_{COLL} denotes the collected charge, τ_{fall} is the collection time constant of the junction (fall time of the current pulse), and τ_{rise} is the ion-track establishment time constant (rise time of the current pulse). The collected charge Q_{COLL} is defined by the particle's *LET* and the charge collection length *L* of the target device, according to relation (2.1). The values of τ_{fall} and τ_{rise} are technology-related. According to [188], τ_{fall} can be expressed in the form,

$$\tau_{fall} = \frac{k\varepsilon_0}{q\mu N_D} \tag{3.2}$$

where *k* is the dielectric constant of silicon (k = 3.9), ε_0 is the permittivity of vacuum ($\varepsilon_0 = 8.85 \times 10^{-12}$ F/m), *q* is the electron charge ($q = 1.6 \times 10^{-12}$ C), μ is the electron mobility, and N_D is the donor concentration. The value of τ_{rise} is usually expressed in terms of τ_{fall} . For example, $\tau_{fall} = 4 \times \tau_{rise}$ in [125] and $\tau_{fall} = 5 \times \tau_{rise}$ in [189]. In general, τ_{rise} is in the range from several ps to tens of ps, while τ_{fall} is from tens of ps to hundreds of ps. The values of τ_{rise} and τ_{fall} can be estimated from TCAD simulations.

Another very common bias-independent current model is the single-exponential model, also known as Freeman's model [190]. It defines the SET current in terms of the total collected charge Q_{COLL} and a technology-related timing parameter τ ,

$$I_{SET}(t) = \frac{2}{\sqrt{\pi}} \frac{Q_{COLL}}{\tau} \sqrt{\frac{t}{\tau}} exp\left(-\frac{t}{\tau}\right)$$
(3.3)

Besides the two aforementioned current models, alternative bias-independent current models reported in literature include: Hu's current model [191], Roche's current model [192, 193], diffusion current model [194], rectangular current model [195], trapezoidal current model [196] and triangular current model [197]. The main difference between these models is related to the level of details regarding the SET current pulse shape. The simplest models, i.e. rectangular, trapezoidal and triangular, are the least accurate but they are easiest for implementation in SPICE/Spectre simulations.

3.3.1.2 Current Models Based on Bias-Dependent Current Source

The main drawback of the bias-independent SET current models is that they consider only the charge collection in a p-n junction with a constant bias [77, 198, 199]. As a result, the simulations with these models cannot reproduce the plateau effect in the current pulse for high LET (see Figure 2.3), and this leads to the swing of SET voltage across the struck node beyond the power supply rails. This phenomenon is physically impossible, and it is known as the voltage overdrive effect. The consequence of this effect is the underestimation of SET voltage pulse width for high values of LET. In reality the voltage across the p-n junction is not constant during the particle strike, but depends on the particle-induced current.

Various modeling approaches taking into account the dependence of node voltage on the SET-induced current have been reported in literature. Some of the common bias-dependent current models have been

proposed by Clark *et al.* [200], Fulkerson *et al.* [201], Hellebrand *et al.* [202], Mavis *et al.* [203], Alvarado *et al.* [204], Kauppila *et al.* [205, 206], and Privat *et al.* [207]. Evaluation on various technologies has proven that the SET current pulse shapes reproduced by bias-dependent current models are very close to those obtained from TCAD simulations. However, the application of these models in electrical simulations is more complex than bias-independent models, because they employ complex mathematical relations and multiple current sources.

Among the existing bias-dependent current models, the model proposed by Kauppila *et al.* has attracted significant interest of the radiation community and has been widely used for characterization of SETs and SEUs in different designs. This model is described by a set of equations, and its implementation consists of a capacitor C_S , one independent current source I_{SRC} and two voltage-dependent current sources G_{REC} and G_{SEE} , as illustrated in Figure 3.5. The capacitor C_S stores the charge which is equivalent to the SET-induced charge, and its value can be chosen arbitrarily. The independent current source I_{SRC} is the standard double-exponential current source, while the two voltage-dependent current sources account for the recombination process and the variation of node voltage due to induced charge. This model can be either integrated in the transistor model or implemented in the circuit simulators as a stand-alone model. The collected charge, particle LET and timing constants (same as for the double-exponential model) are specified as input parameters of the model. Detailed description of this model can be found in [205, 206].

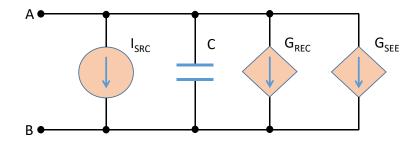


Figure 3.5: Bias-dependent current model proposed in [205, 206]

3.3.1.3 Current Models Based on Two Bias-Independent Current Sources

To resolve the limitations of single bias-independent current models, and provide a simple and easy-to-use alternative to the bias-dependent models, two different approaches employing two double-exponential current sources have been proposed. The use of two double-exponential current sources connected in parallel, instead of a single double-exponential current source, has been proposed by Black *et al.* [208]. By appropriately adjusting the parameters of the current source, a realistic SET current shape with plateau region can be reproduced. A different approach with two current sources, where one source is connected between the transistor's drain and bulk terminals while the other is connected between the bulk and source terminals, was proposed by Kleinosowski *et al.* [209].

3.3.1.4 Current Models Based on Piecewise Interpolation

The piecewise approximation method is used to replace a realistic SET current pulse with a number of segments modeled by simple mathematical relations. Then, the current pulse expressed by the piecewise approximation relations is applied in SPICE/Spectre simulations as a compact model. The most common

approach is the piecewise linear (PWL) approximation, where the SET current pulse obtained from TCAD simulations is represented by a number of linear segments [198, 210]. An alternative approach, based on the piecewise quadratic approximation (PWQ), has been proposed by Dharchoudhury *et al.* [211]. In this case, the SET current waveform obtained from TCAD simulations is represented by a number of segments defined by a second order polynomial.

3.3.1.5 Current Models Based on Look-up Table

The concept of modeling the SET-induced current pulse with a LUT combines the accuracy of TCAD simulations and the speed of circuit simulations [212, 213]. Basically, the idea is to extract the SET current waveforms for different design and operating settings from TCAD simulations or irradiation experiments, and store the obtained data in the LUT. The circuit simulators reconstruct the SET pulses by reading the data from the LUT. In [212], a two-dimensional LUT is constructed by expressing the current values in terms of the node voltage and collected charge, and the LUT readout is performed with a custom-developed SPICE model. The solution proposed in [213] employs the LUT for storing the current values in terms of supply voltage and time.

3.3.1.6 Comparison of SET Current Models

All presented SET current models have both advantages and disadvantages. It is therefore necessary to consider carefully the features of each model in order to determine to what extent it could be applicable for evaluating a particular design. The major advantages and disadvantages of the analyzed SET current models are outlined in Table 3.2. From previous discussion it can be seen that the most accurate representation of the SET pulse width is achieved with the bias-dependent current models. However, implementation of the bias-dependent models in SPICE simulations requires effort in adopting the model to a particular simulation tool and technology. On the other hand, the models based on independent current sources may still provide reasonable results for the analysis of critical charge, and some variants of these models are readily available in SPICE-like simulation tools.

Model type	Advantages	Disadvantages
Single bias-independent current source	Represented with simple analytical models that can be easily applied in circuit simulations	Insufficiently accurate because the bias dependence of SET current is neglected
Bias-dependent current source	The SET current pulse shape is in good agreement with TCAD	Based on complex mathematical relations
Two bias-independent current sources	More accurate than bias-independent models	Complex procedure for deriving the model parameters
Current source based on piecewise interpolation	More accurate than bias-independent models	Device simulations or experiments are required for calibration
Current sources based on look-up table	More accurate than bias-independent and piecewise interpolation models	Device simulations or experiments are required for calibration

3.3.2 Critical Charge Models

The critical charge is an essential metric for assessing the robustness of individual circuit nodes to particle strikes. To estimate the critical charge, simulations with the bias-independent current models are applied. The overdrive effect caused by the bias-independent current models is not a critical issues in this case, because the critical charge analysis considers only the case when the SET voltage pulse crosses the threshold level. Though, it should be noted that the value of critical charge strongly depends on the type and shape of the current pulse [214, 215]. The current pulse is injected in the target circuit node, and by varying the charge over the predefined range, the critical charge is determined as the minimum charge which causes the voltage level across the target node to swing beyond the threshold level (half of supply voltage). In order to avoid timely search of the LUTs with critical charge values, it is desirable to use analytical models. An accurate critical charge model should take into account the impact of all parameters which are relevant in the design phase, such as input logic levels, target gate size, load gate size, supply voltage, operating temperature, parasitic capacitance of interconnections, and timing parameters of the current pulse used in simulations. Simulation studies have shown that the critical charge in most cases decreases or increases fairly linearly when the contributing parameters are varied [214, 215], and this has been utilized as a basis for development of critical charge models. Two modeling approaches have been used: (i) fitting of simulation data, or (ii) analytical derivation of the model by solving the differential equation which describes the SET response of a target circuit node.

The simplest model defines the critical charge of a circuit node as a product of supply voltage V_{DD} and node capacitance C_N ,

$$Q_{CRIT} = C_N V_{DD} \tag{3.4}$$

However, the model defined by the relation (3.4) neglects the impact of restoring current, and does not express explicitly the impact of transistor size and current pulse. As a result, this model is not sufficiently accurate for analysis of real designs.

A modified version of the model defined by the relation (3.4), taking into account the restoring current, has been proposed by Roche *et al.* [192],

$$Q_{CRIT} = C_N V_{DD} + I_R T_{F_i} \tag{3.5}$$

where I_R is the maximum current supplied by the restoring transistor and T_F is the flipping time (the time from the onset of SET current to the change of logic level). An alternative model has been proposed by Xu *et al.* [216] by using the SET current pulse duration T_{PULSE} instead of flipping time T_F . Nevertheless, the model defined by the relation (3.5) is also not an explicit function of contributing parameters.

Jahinuzzamman *et al.* [217] have derived a critical charge model for memory elements by solving a differential equation for the target node and using a double-exponential current source. The model expresses the critical charge in terms of injected charge Q, fall-time constant τ_{FALL} of the double-exponential current pulse and time interval between the start of current pulse and the onset of a bit-flip T_{CRIT} ,

$$Q_{CRIT} = Q \left(1 - e^{-T_{CRIT}/\tau_{FALL}} \right)$$
(3.6)

where T_{CRIT} is a function of the parameters of PMOS and NMOS transistors, and node resistance and capacitance.

Choudhury *et al.* [218] have proposed a model of critical charge in terms of the transistor's W/L ratio, supply voltage V_{DD} , transistor's threshold voltage V_T , load capacitance C_{OUT} , noise margin γV_{DD} and fall time constant of the double-exponential current model τ_{FALL} ,

$$Q_{CRIT} = k(\gamma V_{DD}) \left(\tau_{FALL} (V_{DD} - V_T) \frac{W}{L} \right)^{1/1+\beta} (C_{OUT})^{\beta/1+\beta}$$
(3.7)

where k and β represent the calibration constants for NMOS and PMOS transistors in the target gate, obtained by fitting the results from SPICE simulations.

Rossi *et al.* [219] have defined the critical charge as a linear function of the transistor channel widths of target and load gates,

$$Q_{CRIT} = Q_{CRIT}_{MIN} + a(W_{TG} - W_{min}) + b(W_{TC} - W_{min}) + c(W_L - W_{min})$$
(3.8)

where W_{TG} is the equivalent channel width of the target gate, accounting for the driving conductance, W_{TC} is the equivalent channel width of the target gate, accounting for the load capacitance, W_L is the equivalent channel width of load gate, and W_{MIN} is the minimum channel width for the investigated technology. Q_{CRIT_MIN} denotes the critical charge for minimum sizes of target and load gates, i.e., for $W_{TG} = W_{TC} = W_L = W_{MIN}$. The coefficients *a*, *b* and *c* are technology-dependent constants obtained by fitting the SPICE simulation results. This model has been derived for an inverter as a target gate and a load inverter, and the model parameters for other gates are obtained by mapping each gate to an equivalent inverter.

An alternative approach for critical charge estimation was presented by Zhang *et al.* [194]. Initially, the model for critical current pulse width is derived by employing the piecewise linear modeling, and then the critical charge is expressed as a function of the critical current pulse width. This model is derived from simulations with a rectangular current model, and defines the critical charge in terms of transistor size and magnitude and duration of current pulse. However, the model was tested only on memory elements.

The reported critical charge models [192, 195, 216 - 219] have low relative error, from 2 to 11 %, with respect to SPICE simulations. However, the comparison with SPICE was done only for the set of parameters included in the models. The actual accuracy of each model would be lower because some relevant parameters (e.g. load size, capacitance of interconnections, temperature) have not been considered in each of these models. In addition, some models incorporate technology parameters which are usually not available to designers. For time-efficient and accurate characterization of SER, it is important to use a fairly simple, but accurate and easily applicable critical charge model.

As an alternative to the critical charge concept, Merelle *et al.* [194] have proposed the $I_{MAX} - T_{MAX}$ (amplitude-duration) criterion, defined as the relation between the SET current amplitude I_{MAX} and the corresponding duration of the SET current pulse (T_{MAX}). For predefined T_{MAX} , the I_{MAX} is determined as the current amplitude necessary to cause an SET or an SEU. The advantage of this criterion over the critical charge metric is that it is almost independent of the shape of current pulse used in SET simulations. **Based on the initial findings in [194], we have proposed an analytical model for the amplitude-duration**

criterion in the form of a rational function [MA6]. However, as the proposed model has been derived only for an inverter, further study has to be conducted to evaluate the model for other gates and to fully assess its benefits over the critical charge metric.

3.3.3 SET Pulse Width Models

The width of the SET voltage pulse resulting from the particle-induced current is a key metric for assessing the probability that a generated SET pulse will cause a soft error. Availability of accurate predictive SET pulse width model is of utmost importance, because the SET pulse width cannot be directly measured in radiation experiments. For derivation of the SET pulse width model it is important to use the SET current model which does not exhibit the voltage overdrive effect. Numerous analytical SET pulse width models have been proposed. As discussed in Chapter 2, the SET pulse shape is defined by a wide range of parameters, and considering the impact of all parameters in a single model is often very challenging. Similarly to the critical charge models, the SET pulse width models can be derived analytically or by fitting the results obtained from current injection simulations.

Most reported SET pulse models are derived using the double-exponential current model. By solving the first order differential equation for the SET response of a circuit node induced by the double-exponential current pulse, Wirth et al. have derived an RC model for the SET amplitude and width in terms of the node resistance and capacitance, supply voltage, fall time constant of the current pulse and time between the onset of SET pulse and its peak [220]. Using a similar RC modeling approach, Rohani et al. [221] have expressed the SET pulse width as a linear function of the node's resistance and capacitance, and the timing parameters of current pulse. An alternative RC model has been presented by Mohanram et al. [222], as a closed-form analytical expression which defines the SET pulse width as a linear function of gate fan-out, collected charge and gate's driving strength. In contrast to the previous models which are based on linear RC modeling, an analytical SET pulse width model in terms of transistor's drain current has been introduced by Garg et al. [223]. Alternatively to analytical modeling, Wang et al. have proposed an SET pulse width model derived by fitting the data obtained from current injection simulations [225]. Their model has been derived for an inverter, and it defines the SET pulse width in terms of the deposited charge and transistors' channel width. In contrast to SET pulse width models, Rao et al. have established a model for the SET pulse shape, employing the Weibull fitting and using the single-exponential current source to characterize the SET pulse shapes for standard gates [175].

All aforementioned SET pulse width models have a common limitation – **they have been derived using the bias-independent SET current models**. Due to the overdrive effect, these models result in significant underestimate of the SET pulse width for large values of injected charge (or LET). Although low relative errors with respect to SPICE simulations have been reported for all models, similarly to the critical charge models this is due to the fact that the models have been validated only for parameter ranges used during the model derivation. Several works have addressed the SET pulse width modeling taking into account the bias-dependence of the SET current. For example, Saremi *et al.* [226] and Bindu *et al.* [227] have proposed the physics-based SET pulse width models which incorporate the technology and material parameters. On the other hand, simpler SET pulse width models based on design parameters have been proposed by Kobayashi *et al.* [227] and Assis *et al.* [180].

In [227], Kobayashi *et al.* have defined a model for calculating the SET voltage pulse width in terms of deposited charge Q_{DEP} and restoring current $I_{RESTORE}$, considering a realistic SET current pulse shape with the plateau region. The model has been derived for SOI CMOS technology. It defines two regions, for low Q_{DEP} and high Q_{DEP} , as follows,

$$T_{SET} = \begin{cases} a \cdot ln\left(\frac{Q_{DEP}}{I_{RESTORE}}\right), & for high Q_{DEP} \\ \\ b \cdot Q_{DEP} \cdot ln\left(\frac{1}{I_{RESTORE}}\right), & for low Q_{DEP} \end{cases}$$
(3.9)

Nevertheless, the model of Kobayashi *et al.* does not express explicitly the relationship between the SET pulse width and the design/operating parameters such as gate size, load size and supply voltage. As a result, this model is not readily applicable for circuit analysis, but requires further characterization in order to include all relevant contributing parameters.

Assis *et al.* [180] have proposed an SET pulse width model derived using a physics-based SET current model and SPICE simulations. The model expresses the SET pulse width at the gate's output as the product of a reference SET pulse width, a restoring current factor and a load capacitance factor, as follows,

$$T_{SET} = PW_{MIN}(Q_C) \cdot R_{CURRENT}(R_T) \cdot C_{LOAD}(C_L)$$
(3.10)

where $PW_{MIN}(Q_C)$ is the reference SET pulse width obtained for the smallest gate, $R_{CURRENT}$ factor describes the effect of transistor resistance network connected to the output node, and C_{LOAD} factor accounts for the impact of capacitance on the SET pulse width. The values of these factors are obtained from SPICE simulations and stored in LUTs. The model has been verified for several scaled technologies and it has been shown that the relative error compared to SPICE simulations is less than 10 % in all cases. The advantages of this model is that it can be extended to include the pulse quenching effect, and the derivation requires only the simulations for inverter. However, the coefficients for other gates are obtained by mapping each gate to equivalent inverters, which is not sufficiently accurate approach for complex gates. In addition, the model does not express explicitly the impact of various contributing parameters.

As the models proposed by Kobayashi *et al.* and Assis *et al.* take into account the bias-dependence of the SET current pulse, they are more accurate than the models based on bias-independent current. However, the aforementioned drawbacks motivate further research on the SET pulse width modeling. In particular, an enhanced SET pulse width model should consider the bias-dependence of the SET current pulse, but also the impact of all relevant design and operating parameters.

3.3.4 SET Propagation Models

The propagation of the generated SET pulse through the circuit is affected by the electrical, logical and timing masking effects, and the PIPB effect. As every gate in the path may cause either broadening or shrinking of an SET pulse, the characterization of SET propagation through a single gate is a precondition for the analysis of SET propagation through the entire combinational path. The variation of the SET pulse amplitude and width during propagation through a single gate depends on the initial amplitude, width and

polarity of the SET pulse, and the propagation delay of the gate. On the other hand, the propagation delay of logic gates is defined by the type and driving strength of the target gate, load capacitance (fan-out), supply voltage and operating temperature. Although both amplitude and width of an SET pulse may vary during the propagation, the variation of the SET pulse width is considered as a more critical parameter because it directly determines the electrical and timing masking probabilities.

In general, the SET pulse will be electrically masked if its amplitude is lower than the threshold voltage level (half of supply voltage), or if its duration is shorter than the propagation delay τ_p of subsequent logic gate. Based on these facts, Omana *et al.* [228] have defined approximate conditions for SET propagation, which states that the SET pulses wider than $2\tau_p$ will propagate without attenuation, while those wider than τ_p but shorter than $2\tau_p$ will propagate with certain attenuation. Employing a similar approach, Dhillon *et al.* defined the SET pulse width at the gate's output T_{SET_OUT} in terms of the input SET pulse width T_{SET_IN} and the gate's propagation delay τ_p as [128],

$$T_{SET_OUT} = \begin{cases} 0, & T_{SET_IN} < \tau_p \\ 2(T_{SET_IN} - \tau_p), & \tau_p < T_{SET_IN} < 2\tau_p \\ T_{SET_IN}, & T_{SET_IN} > 2\tau_p \end{cases}$$
(3.11)

However, the models of Omana *et al.* and Dhillon *et al.* do not consider explicitly the impact of supply voltage and input levels. Moreover, these models neglect the SET pulse broadening effect, as well as the polarity and rise and fall time delays of the input SET pulse.

Wirth *et al.* [229] have proposed a model considering the dependence of output SET pulse width T_{SET_OUT} on input SET pulse width T_{SET_IN} , propagation delay of the logic gate τ_p , and difference between the high-to-low and low-to-high transition times $\Delta \tau_p$. The model is divided into four regions,

$$T_{SET_OUT} = \begin{cases} 0 & T_{SET_IN} > k\tau_p \\ (T_{SET_IN}^2 - \tau_p^2)/T_{SET_IN} & (k+1)\tau_p > T_{SET_IN} > (k+3)\tau_p \\ (k+1)\tau_p (1 - e^{k - T_{SET_IN}/\tau_p}) + \Delta\tau_p & k\tau_p > T_{SET_IN} > (k+3)\tau_p \\ T_{SET_IN} + \Delta\tau_p & T_{SET_IN} > (k+3)\tau_p \end{cases}$$
(3.12)

where k is the fitting coefficient which depends on technology, and it is constant for all gates in a given library. First region denotes the scenario when the SET pulse is filtered out. Second and third regions correspond to the cases when the SET pulse is degraded. Fourth region denotes the situation when the SET pulse is not degraded, but either broadening or shrinking occurs (depending on the value of $\Delta \tau_p$).

Gili *et al.* [230] have derived a model of the output SET pulse width T_{SET_OUT} in terms of the input SET pulse width T_{SET_IN} , defined by the relation,

$$T_{SET_OUT} = a \cdot T_{SET_{IN}} + t_o \cdot e^{-\frac{T_{SET_{IN}}}{t_i}} + b$$
(3.13)

where *a* and *b* are fitting parameters expressed as linear functions of the amplitude of input SET pulse. The value of *a* was found to be constant for all investigated gates, while *b* is extracted for each gate. The values of t_o and t_i represent the timing parameters and are constant for all gates in a given technology.

Rajaraman *et al.* [174] have proposed a model that expresses the output SET pulse width as a function of the input SET pulse width, transition delay and pulse amplitude,

$$T_{SET \ OUT} = (T_{SET \ IN} - d_1) + X \cdot d_2 \tag{3.14}$$

where d_1 and d_2 are the first and second transition delays of the output pulse, respectively. X is the scaling factor dependent on polarity of input pulse.

Hamad *et al.* [90] have characterized the SET propagation effects in standard logic cells considering the minimum SET pulse width that can propagate through a gate (denoted as *SET_weak*) and the Load Input Combination Factor (*LICF*) which accounts for the load impact. This work also takes into account the input levels, SET pulse polarity and fan-out. The *SET_weak* and *LICF* values are extracted for each standard cell and stored in respective LUTs. Consequently, for any input SET pulse width larger than *SET_weak*, the output SET pulse width is obtained as,

$$T_{SET OUT} = T_{SET IN} \pm LICF \tag{3.15}$$

where + *LICF* denotes the pulse broadening and - *LICF* denotes the pulse attenuation. For each gate, the pulse broadening or attenuation depends on the input polarity of the SET pulse.

Using the presented models allows for predictive assessment of SET attenuation or broadening during propagation through a single logic gate. Given the initial SET pulse width, the electrical masking and SET broadening in a combinational path can be estimated by analyzing successively each gate in the path. While these models provide faster analysis than the LUT-based approaches, their accuracy is the main drawback. That is the result of the fact that none of the reported models takes into account all relevant parameters affecting the SET propagation. For example, **the impact of supply voltage and operating temperature are neglected in all models**, which may result in significant errors in the SER computation. A detailed characterization of SET propagation was performed in [134, 181]. However, the characterization data was stored in LUTs, and no analytical propagation model was established. Considering the above mentioned shortcomings of the existing models, it is necessary to establish an improved analytical model that will express the propagation-induced variation of SET pulse width in terms of parameters that have dominant contribution to the SER, and that are directly used in the design process.

3.4 Gate-level SET Mitigation Approaches

Due to heterogeneous structure of combinational circuits and analog nature of SETs, protecting the combinational logic may be very expensive in terms of introduced area, delay and power overhead. It is therefore imperative to select the mitigation strategy which can provide a reasonable compromise between the desired SER and the introduced overheads. To achieve sufficient radiation hardness at minimum cost, the SET mitigation needs to be considered at multiple levels of abstraction, as defined by the general rad-hard design flow depicted in Figure 3.1. Traditional approach for SET mitigation in combinational logic is based on hardware replication in the form of N-tuple Modular Redundancy (NMR), where N replicas of the target circuit are created, and a majority voter is employed to select the correct output value [231]. One the most versatile NMR schemes is the Triple Modular Redundancy (TMR) [53]. While the TMR is effective in mitigation of SETs, the area and power overhead of more than 200% are not acceptable for cost-constrained applications. Moreover, the majority voter is sensitive to SETs. A TMR variant with four voters has been introduced to mitigate double errors resulting from a single particle strike, but the area and power overhead remain as critical issues [232]. The area overhead of standard TMR can be reduced by protecting only a subset of input signals [233], or by employing the approximation-based TMR [234]. Another low-cost alternative is the Dual Modular Redundancy (DMR) with a guard gate (C-element) as a majority voter [235, 236]. Furthermore, the error detection and correction methods [237 - 239], combining the error detection in combinational logic with the error correction in sequential logic (or the use of fault-tolerant sequential logic), may provide over 20 % area and power savings compared to TMR. Instead of using hardware redundancy, the SETs can be mitigated with temporal redundancy. A typical approach is the double-sampling, where the outputs of a combinational circuit are sampled at two different instants to detect the errors, and additional logic is employed for error correction [235]. Another well-known temporal redundancy scheme is based on the insertion of delay elements in the data path, such that all SETs shorter than the predefined delay are masked [203]. However, the main drawback of temporal redundancy is high performance penalty (delay overhead). A cost-effective alternative to the aforementioned techniques is the gate-level SET mitigation, aimed at the reduction of the SET sensitivity of individual gates in sensitive logic paths.

The key rationale for gate-level SET mitigation is that it can provide significant SER reduction by protecting a subset of the most sensitive gates. Namely, it is not necessary to harden every gate in the circuit since the logic gates in any circuit have differing impact on the total SER, and only a fraction of them has dominant contribution to the total SER. As the sensitivity of each gate depends on input logic levels, due to logical masking only a subset of gates or logic paths will be sensitive during most time of the circuit operation. It was shown that around 50 % of gates in ISCAS89 benchmark circuits contribute to over 80 % of combinational soft errors [240]. Furthermore, for critical circuits such as the clock and reset trees, the gate-level hardening is the most effective solution, because the replication of complete circuit would result in very high area and power overhead. Numerous studies have confirmed that selective gate-level mitigation provides an acceptable trade-off between the SER improvement and the overheads. Selective gate-level mitigation involves two phases: (i) identification of the most sensitive gates in the circuit (i.e., gates with largest SER), and (ii) application of mitigation measures to the most sensitive gates to reduce the overall SER. The main goals of gate-level SET mitigation are to:

- *Reduce the SET generation probability* by increasing the critical charge of sensitive gates (i.e., by increasing the gate's capacitance and drive strength to enable faster dissipation of induced charge).
- *Reduce the SET propagation probability* by enhancing the capability of logic gates to electrically mask the incoming SET pulses, and/or by inserting dedicated SET filtering structures at the outputs of combinational paths.

Generally, the gate-level hardening can be achieved by: (i) modifying the internal structure of existing gates, or (ii) using existing gates which are inherently more robust to SETs, or adding local redundancy to enhance their robustness. Some typical hardening techniques based on modification of the gate's internal structure include: asymmetric transistor sizing [241], transistor folding [242], transistor reordering (arrangement of transistors in the cell) [243], and insertion of sleep transistors [244]. Although these techniques can mitigate the SETs with minimum overhead, they require significant effort because it is necessary to

redesign the existing logic gates and then fully characterize them, while in some cases might be required to modify the standard design flow in order to allow the implementation of new gates. On the other hand, the hardening based on the use of existing standard cells is more time-efficient and can be accomplished with the standard IC design tools and flows. For that reason, this work addresses the gate-level techniques which do not require the redesign of standard cells.

A variety of gate-level design styles for hardening of standard combinational gates without modifying their internal structure have been reported in literature. In general, the gate-level SET hardening of standard combinational gates can be accomplished by: (i) replacing a target gate with a larger gate or another type of gate with higher SET generation or propagation robustness, (ii) replication of a target gate, and (iii) connection of redundant logic to the output of a target gate. The key features of the most common techniques, with emphasis on their benefits and limitations, are described in the following.

3.3.5 Gate Upsizing

The most popular gate-level SET mitigation technique is the symmetric gate upsizing [109, 125, 128, 245], i.e., replacement of a smaller gate with a larger one, as illustrated in Figure 3.6. As a result of gate upsizing, the critical charge of all nodes is increased. It was shown in [109] that by upsizing 10 % of the most sensitive gates in ISCAS85 benchmark circuit, the total SER can be reduced by more than 40 %. However, due to the increase of sensitive area, the impact of gate upsizing on SER is limited. According to Rezaei *et al.*, the gate upsizing can lead to a decrease of SER up to a certain threshold beyond which any further increase in gate size would not cause changes in SER [133]. Similarly, based on irradiation tests on logic chains in 90 nm technology, Cannon *et al.* have shown that the upsizing is not effective at high LET, i.e., larger gates may have larger SER than the smaller gates [246]. That is because large sensitive area dominates over driving strength at high LET. Moreover, due to the reduced SET filtering capability of larger gates, the gate upsizing is not sufficient for SET mitigation in logic paths where the PIPB is likely to occur.

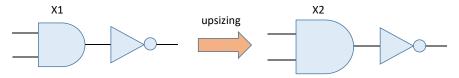


Figure 3.6: Gate upsizing by replacing AND2_x1 with AND2_x2

3.3.6 Gate Duplication/Cloning

Gate duplication (also known as gate cloning) [247, 248] is a common alternative to gate upsizing. The idea behind this approach is to replace a single gate with two gates of the same type with connected inputs and outputs, as illustrated in Figure 3.7 (a). In such a way, the critical charge of the gate is increased without affecting its logic function. Besides, using a duplicate of two gates with lower driving strength instead of a single gate with higher driving strength contributes to better SET filtering. Nevertheless, this approach results in larger area than the gate upsizing because of spacing between the gates and additional wiring. Garg *et al.* [249] have proposed a modification based on inserting a clamping device between the original gate and its copy (clone), as illustrated in Figure 3.7 (b). Two diodes are used as the clamping devices. The clamping devices turn on when a particle-induced voltage glitch is sufficiently large. As demonstrated in

[249], this approach introduces the delay overhead per gate of around 1.76 %, and the area overhead per gate of around 277 % for selected benchmark circuits. However, the need for different supply voltage levels for original gate and its copy complicates the power supply design.

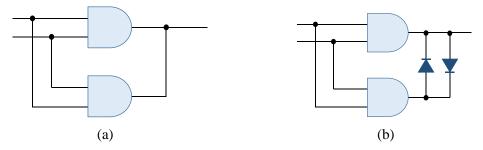


Figure 3.7: Duplication of AND gate: (a) standard variant, and (b) variant with clamping diodes

3.3.7 Load Upsizing

Increasing the load size is another possible approach for hardening a sensitive combinational gate. This can be achieved by using load gates with higher driving strength, as shown in Figure 3.8. However, as shown in [250], the upsizing of a load gate produces less than 50 % increase in critical charge, while gate upsizing can increase the critical charge several times. Unlike gate upsizing, the load upsizing improves only the SET robustness of the gate's output node. It was shown in [128] that the suppression of generated SET pulse can be achieved only with very large load capacitance. Nevertheless, the advantage of load upsizing is low area and power overhead. The combination of load upsizing, gate upsizing and supply voltage adjustment can provide almost 80 % SER reduction with modest area and power overhead [128].

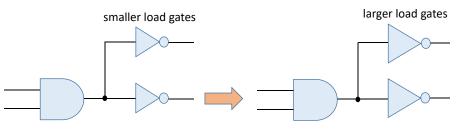


Figure 3.8: SET mitigation by increasing the size of load gates

3.3.8 Guarded Dual Modular Redundancy

Although hardware replication is typically applied at the circuit or system levels, it may be also applied to individual gates. The gate-level DMR and TMR approaches have been investigated in [251]. It was shown that DMR with guard gates, denoted as Guarded DMR (GDMR), provides better performance than gate-level TMR in terms of area, delay and power overhead. In Figure 3.9, a GDMR version of AND gate is illustrated. The guard gate consists of four stacked transistors, and its output will change only when both inputs have the same logic level. Thus, an SET induced in one gate will not propagate to the output. Use of a guard gate also allows to filter short SETs arriving at the inputs, and provides immunity against double SETs if the target gates are sufficiently spaced. Because the guard gate inverts the signal, an inverter is required at the output node. The main drawbacks of GDMR are high area overhead per gate (over 100 %), and additional sensitive nodes (guard gate and inverter).

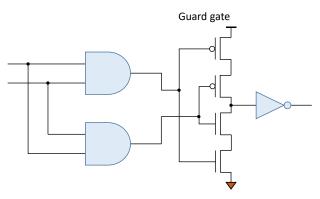


Figure 3.9: GDMR implementation of AND gate

3.3.9 Insertion of Charge Sharing Logic

The SET robustness of a logic gate can be enhanced by connecting redundant dummy logic to its output [252], as shown in Figure 3.10 (a). Insertion of redundant logic increases the gate's output capacitance, and thus facilitates the dissipation of particle-induced charge, and enhances the SET filtering. The redundant logic can be realized with a number of inverters whose inputs are connected to the target node, while their outputs are hardwired and left to float, or connected to a dummy gate (e.g. AND). With a larger number of inverters, the critical charge of the target node will be larger, but the SET pulse width generated at the target node will also be larger because of increased node capacitance. Evaluation on FPGA has shown that this approach has zero-delay overhead [252], but the area overhead per gate may not be negligible.

3.3.10 Insertion of Cross-Coupled Inverters

Another SET mitigation approach is based on the connection of two cross-coupled inverters to the gate's output node [253], as illustrated in Figure 3.10 (b). Alternative approach has been proposed in [254], where the cross-coupled inverters are connected between the output of one gate and the input of the following gate. The cross-coupled inverters act as a capacitor. The critical charge at the gate's output node is increased due to the increase of capacitance, and the SET filtering capability is enhanced since the added capacitive element acts as a low-pass filter. However, the key limitation of this approach is that the minimum sized inverters have to be used in order to avoid the degradation of normal signal, which limits the impact on the increase in critical charge.

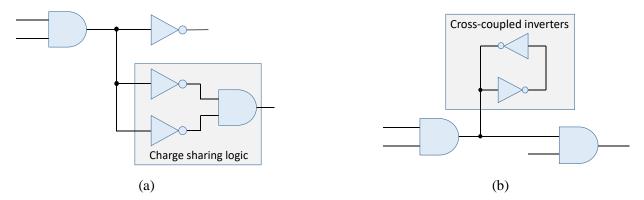


Figure 3.10: SET mitigation in AND gate with: (a) charge sharing logic, (b) cross-coupled inverters

3.3.11 Insertion of Schmitt Trigger

Due to its inherent hysteresis property, which is useful for enhancing the noise immunity, the Schmitt trigger may be also used for SET filtering [255, 256]. A typical configuration of Schmitt trigger is illustrated in Figure 3.11 (a). By inserting the Schmitt trigger in the logic path, the noise margin is increased, allowing to filter the SET pulses with amplitude below a certain threshold level (defined by the transistor sizes in the Schmitt trigger). However, only short SETs whose amplitudes are lower than the supply voltage level may be filtered. The main drawback of this technique is that it adds more transistors than other techniques, which results in larger area and power overhead.

3.3.12 Insertion of Transmission Gate

An alternative SET filtering configuration employs a transmission gate composed of PMOS and NMOS transistors, as illustrated in Figure 3.11 (b) [257]. The transmission gate acts as a low pass filter, enabling to attenuate or completely filter short SET pulses propagating through the path. A modified version with inverters at the input and output of transmission gates is proposed in [258]. By connecting the gate of PMOS transistor to ground, and the gate of NMOS transistor to supply voltage, the transistors in the transmission gates will always be in conductive state. Using larger transistors or cascading multiple transmission gates increases the filterable SET pulse width. As demonstrated in [258], two transmission gates can filter the SETs up to 60 ps, while four stages can filter the SETs up to 132 ps. However, increasing the filterable SET pulse width leads to a linear increase of propagation delay. In addition, because the transistors are always conducting, the power overhead may be significant.

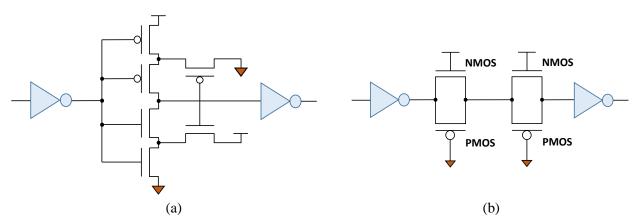


Figure 3.11: SET mitigation with: (a) Schmitt trigger, and (b) transmission gates

3.3.13 Insertion of Guard Gate Filter

One of the most widely used approaches for SET mitigation is based on a filter composed of a guard gate and a delay element [259, 260], illustrated in Figure 3.12 (a). This approach is typically applied at the primary outputs of combinational logic (inputs of flip-flops), but it can also be applied for in-circuit SET filtering. The filterable SET pulse width is equivalent to the value of delay. Since the guard gate's output changes only when both inputs are at the same logic level, all SET pulses shorter than the predefined delay will be filtered. The benefit of this configuration is that is can be designed to filter any SET pulse width. As the SET pulse widths are from dozens of ps to several ns, an ideal SET filter should be capable of filtering the SETs longer than 1 ns. However, suppressing long SETs induces significant delay penalty, which could be unacceptable for many applications. In addition, the weak point of the delay-based filter is that the guard gate is sensitive to SETs. Since the guard gate inverts the signal, an inverter has to be added at the output, which also increases the sensitivity to SETs.

3.3.14 Insertion of Cascaded Inverters

The SET filtering can be achieved by inserting two cascaded inverters in a logic path, where the first inverter is significantly larger than the second, as shown in Figure 3.12 (b). As demonstrated in [146], the use of a combination of inverters with sizes 0.5x and 32x provides very good suppression of short SET pulses, while reducing the size of the second inverter weakens the filtering capability. However, the introduced power overhead may be large (over 50 %) [146]. Instead of two cascaded inverters, a single standard buffer can be used. However, standard buffers available in digital libraries are composed of two inverters where one inverter is 2 - 3 times larger than the other, which is not sufficient for effective SET filtering.

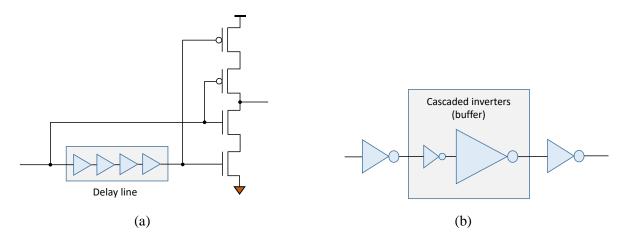


Figure 3.12: SET mitigation with: (a) delay element and guard gate, (b) two cascaded inverters

3.3.15 Comparison of Gate-level SET Mitigation Techniques

The main advantages and disadvantages of the gate-level SET mitigation techniques analyzed in previous discussion are summarized in Table 3.3. As can be observed, there is no an optimal solution, since every technique incurs penalties in terms of area, delay and power overheads. In addition, the gate-level solutions provide limited improvement in either SET generation or SET propagation, but usually do not address both aspects efficiently. Due to the limitations of each technique, it is not effective to use a single technique for the selective hardening, as this would result in the over-design. For instance, by upsizing the most sensitive gates, their robustness will be enhanced but this will not suppress the SETs propagating through these gates. On the other hand, inserting the SET filters at the primary outputs of the circuit is not economical because some paths may have low SET sensitivity, and for critical paths the SET filters may violate the timing constraints. Therefore, the most effective solution is to combine multiple techniques in order to leverage their complementary advantages.

Several works have investigated the use of multiple gate-level hardening techniques to achieve the compromise between radiation hardness and area, delay and power overheads. A well-known solution is

the combined use of gate sizing and gate duplication (cloning) [248]. This concept is useful in designs with a large number of diverging paths, where the advantage of gate duplication for SET filtering may be useful. However, this approach does not provide optimal results from the aspect of SET filtering. A combined application of cross-coupled inverters, gate resizing and gates with low threshold voltage has been explored in [253]. However, the cross-coupled inverters must be designed with the minimum sized inverters and the low threshold voltage gates may not be available in every standard library. Furthermore, the combination of gate sizing and selection of flip-flops with enhanced temporal masking has been proposed in [245], but this methodology does not resolve the limitations of the gate sizing technique. The combined application of gate sizing, insertion of transmission gate and dual supply voltage is another possible approach [258]. Furthermore, the upsizing of target and load gates, together with the adjustment of supply voltage and transistors' threshold voltage, has been investigated in [128].

SET mitigation technique	Advantages	Disadvantages
Gate upsizing	Significant improvement of robustness to direct particle hits	Weak impact on SET filtering (electrical masking)
<i>Gate duplication (with or without clamping)</i>	Improvement in SET robustness similar to gate upsizing but with better SET filtering	Larger area compared to gate upsizing
Load upsizing	Low overhead	Moderate improvement of SET robustness
Guarded DMR	Significant improvement of robustness to direct particle hits	Large area overhead per gate, and additional sensitive nodes
Insertion of charge sharing logic	Negligible delay overhead	Large area overhead per gate
Insertion of cross-coupled inverters	Filtering of short SETs	Only minimum sized inverters can be used
Insertion of Schmitt trigger	Filtering of short SETs	Large area and power overhead
Insertion of transmission gates	Filtering of short SETs	Large power overhead
Insertion of guard gate filter	Possibility of filtering long SETs	Additional sensitive nodes
Insertion of cascaded inverters	Filtering of short SETs	Large power overhead

Table 3.3: Comparison of gate-level SET mitigation techniques

Although all above mentioned combinations of SET mitigation techniques provide significant SER reduction with area and power overhead below 50 %, these approaches have been verified only for a limited number of test circuits. To the best of our knowledge, **there is no a published report on the systematic characterization of all aforementioned SET mitigation techniques, considering the quantitative gain of each technique in terms of SET generation and propagation, and the quantitative loss in terms of introduced overheads**. Moreover, most of the reported techniques do not fully comply with the relevant SET sensitivity models, i.e., the increase in SET robustness due to the application of a particular gate-level

mitigation technique cannot be evaluated with the existing SET models. To address these issues, the gatelevel mitigation techniques should be evaluated for each gate in the standard library, and this should be done as an integral part of the standard library characterization. Moreover, to address the limitations of existing gate-level SET mitigation techniques, it is necessary to explore new solutions and methodologies for combined application of multiple techniques.

3.5 Particle Detectors for On-line Soft Error Rate Monitoring

The gate-level hardening, combined with the circuit- and system-level techniques, can provide efficient soft error mitigation in a complex design. However, if the hardening measures are static (fixed) at all abstraction levels, the resulting penalties (area, delay and power overhead) would be prohibitively high. For example, in space missions, the fault tolerance requirements are variable because the system SER varies depending on radiation conditions. It is therefore not practical to exploit the system resources for radiation hardening when the SER is low (under low radiation exposure). A cost-effective approach is to employ the adaptive fault tolerance, i.e., to activate the fault tolerance mechanisms only when they are required. In that regard, the hardening of a complex system is accomplished by combining the static and dynamic techniques, whereby the gate-level measures are applied as static, while the higher-level (mainly the system-level) measures such as TMR are applied in a dynamic fashion.

To apply the adaptive fault tolerance, the sensory hardware for monitoring the variation of parameters affecting the system's SER is required. In general, the soft error detectors sense either SETs or SEUs induced by incident energetic particles. For comprehensive analysis of the radiation environment, the soft error detectors should detect both the particle flux and the LET. Moreover, the detectors should be have sufficiently large sensing area in order to ensure high sensitivity to incident particles, and should be robust to faults that may be induced by external sources or caused by the change of operating conditions. Although the particle detectors are implemented as stand-alone units in many applications, for a self-adaptive system it is preferable to have *in-situ* monitoring, i.e., the particle detectors should be integrated on the same chip with the target system in order to sense the radiation conditions to which the system is exposed. However, the particle detectors and related processing logic increase the chip area and power consumption. Therefore, the design of soft error monitors should be carefully planned for a target technology and system.

Depending on the design and operating principles, the particle detectors can be categorized into five main types: (i) bulk built-in current detectors, (ii) acoustic wave detectors, (iii) diode detectors, (iv) static random access memory (SRAM)-based detectors, and (v) 3D NAND flash detectors. The main features of each detector type are briefly described in the following.

3.5.1 Bulk Built-in Current Detectors

Since the energetic particles induce the current pulses in a target circuit, the use of current sensors is a common approach for detecting these events. A simple design of a current detector for detection of energetic particles was proposed in [261]. This detector was connected to the power supply rail of SRAM. However, this solution was not suitable for detection of particle strikes in combinational logic because of difficulty to differentiate the signal induced by a particle from the normal signal. An improved current sensor, known

as the Bulk Built-in Current Sensor (BBICS), was proposed in [262, 263]. Instead of connecting to supply rail, the BBICSs are connected to the bulk terminal of respective transistors. Separate BBICSs are needed for PMOS and NMOS transistors. A design of a simple BBICS for PMOS transistors (PMOS_BBICS) [263] is illustrated in Figure 3.13 (a), and the connection of two BBICSs to an inverter is illustrated in Figure 3.13 (b). For NMOS_BBICS, NMOS transistors are used instead of PMOS transistors. When the bulk current exceeds the threshold level, a flag signal (SET indication) is generated by the detector, allowing to trigger the soft error correction mechanisms. Various BBICS implementations with different number of transistors have been reported [264 – 266], and more complex implementations offer better performance.

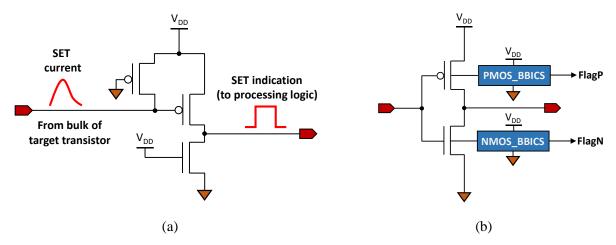


Figure 3.13: BBICS implementation: (a) design of a PMOS-BBICS, and (b) connection of two BBICSs to an inverter [263]

The major advantage of BBICSs is the possibility to provide the information on faulty locations (strike locations), since they are connected directly to the target circuit. This enables to activate the error correction mechanisms only within the affected subcircuit. The low-power consumption, mainly related to the leakage current, is another important feature of BBICSs. Moreover, it is not necessary to connect a sensor to each transistor, but one sensor can be utilized to monitor tens or thousands of transistors [262, 263]. This can be used as a guideline in planning the number and spatial distribution of BBICS on a chip, in order to achieve high detection efficiency with a minimum number of sensors.

Nevertheless, the application of BBICS is associated with limitations. The key disadvantage of reported BBICS implementations is that only the strike locations in the target circuit can be detected, but the information on the particle flux cannot be obtained directly. As the BBICSs are distributed across the chip, it is necessary to implement additional logic for collecting data from all sensors and calculating the error rate from which the particle flux can be determined. However, there are no reports on such implementations. Although it could be theoretically possible to detect the LET with BBICS, e.g. in terms of the width of SET indication signal, no previous reports have analyzed such a possibility. In addition, the laser experiments performed on one version of the current detector [267] have revealed that BBICS sensitivity deteriorates with the increasing number of monitored transistors. A possible improvement by using the triple-well CMOS has been proposed [268], but this is not applicable to technologies with one or two wells. Moreover, as the BBICSs are connected to the target logic, they may be prone to other noise sources (e.g. substrate noise), which could lead to the triggering of false alarms.

3.5.2 Acoustic Wave Detectors

A particle strike can generate intense acoustic waves in the substrate of the target circuit. For detecting such waves, the acoustic wave detector can be employed [269, 270]. A typical implementation of an acoustic wave detector is based on a cantilever-like structure, as illustrated in Figure 3.14 [270]. The cantilever acts as a capacitor, and the acoustic waves induced by the particle strikes cause the change of the capacitance. Thus, by measuring the capacitance of the cantilever, the particle strikes can be sensed. For this purpose, the mixed-signal processing is needed.

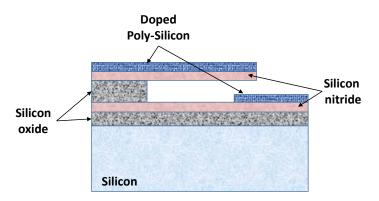


Figure 3.14: A cross-section of cantilever structure for acoustic wave detection [270]

The detector proposed in [270] can be fabricated in CMOS technology, allowing easy integration into standard ICs. A single cantilever structure occupies the area of around 1 μ m², which is roughly the area of an SRAM cell in 45 nm CMOS technology [270]. In order to achieve a sufficiently large sensing area, multiple detectors need to be distributed on the chip. Generally, using a larger number of detectors enables faster detection. Proper dimensioning of the acoustic wave detector and choice of an appropriate number of detectors for the target chip is essential for achieving high sensitivity to particle strikes. Detailed guidelines for choosing the detector dimensions and calibrating the detector are given in [270].

Similarly to BBICS, the spatial distribution of acoustic wave detectors on the chip offers the possibility to detect the exact location of particle strikes. The strike location is estimated based on the algorithm that computes the relative time difference of arrival of acoustic waves to different detectors [270]. However, to the best of our knowledge, there is no a report on the performance of these detectors under real radiation exposure. Furthermore, as the detector reacts to acoustic waves, it may be prone to false alarms due to the acoustic waves from non-radiation sources. Also, for measuring the particle flux and LET it is necessary to employ more complex processing circuitry.

3.5.3 Diode Detectors

The *p*-*n* junctions (diodes) are among the most widely used type of particle detectors [271 - 273]. They are operated in reverse bias to achieve minimum leakage current and maximum depletion layer width, thus ensuring high detection efficiency. Higher sensitivity can be obtained by using PIN instead of PN diodes, since PIN diodes have an intrinsic layer between P and N layers which increases the sensing volume. In a practical implementation, multiple diodes are connected in the form of strip or pixel detectors to obtain

larger sensitive area. As a result of a particle strike in diode, a current pulse is generated. Measuring the induced pulsed current enables to acquire the complete information on the radiation exposure and determine with high accuracy the induced charge, particle flux and LET spectra.

However, the use of diode-based detectors for the purpose of triggering the dynamic fault tolerance mechanisms in an IC may be too costly because different technologies may need to be combined. Namely, the diodes are usually not manufactured in the same technology as the target system, which makes it challenging to integrate them on the same chip. Moreover, the diode detectors require complex mixed-signal processing, which increases the overall cost of implementation. A typical processing logic for a single diode is composed of a charge sensing amplifier (CSA), a pulse shaper and an analog-to-digital converter, as illustrated in Figure 3.15. As the practical implementations may be composed of hundreds or thousands of diodes, the hardware and power overhead due to processing circuitry may be too high.

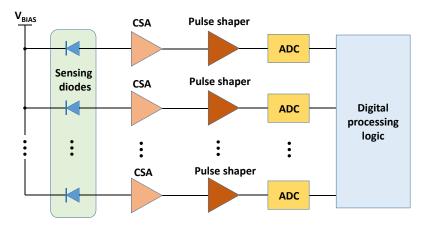


Figure 3.15: Diode detectors with readout circuit

3.5.4 SRAM Detectors

The use of commercial or custom-designed SRAMs as high-energy particle detectors, implemented as stand-alone ICs, has proven to be a very useful solution for soft error monitoring in terrestrial and space applications [274 - 277]. The operation principle is based on counting the number of SEUs in SRAM cells. When a particle hits a sensitive transistor within a cell, and deposits a certain amount of charge exceeding the critical charge, the respective logic state will flip from 0 to 1 or vice-versa. The sensitivity is proportional to SRAM size (number of SRAM cells). The most common implementations employ the well-known six-transistor (6T) cells. Based on the number of SEUs and the cross-section of SRAM obtained experimentally, the particle flux can be calculated from the relation (2.6) given in Section 2.4.4. The SEUs are detected and corrected using appropriate Error Detection and Correction (EDAC) mechanisms and memory scrubbing. The detection latency depends on the scrubbing period that is defined by the clock frequency.

The main advantages of SRAM-based detectors are very simple operating principle, no need for analog processing and possibility of manufacturing in the same technology as the standard ICs. However, this type of detector has several crucial limitations. In stand-alone implementations [274 – 277], the area overhead due to the EDAC logic may be too large. The EDAC techniques suffer from the limitation in the number of detectable and correctable errors, which may lead to the error accumulation as a result of multiple upsets.

Moreover, due to scrubbing the response of SRAM detectors may be in the order of ms, which is slower compared to other detector types. As a low-cost alternative to stand-alone SRAM detectors, an embedded SRAM detector with negligible area overhead of less than 1 % has been proposed recently [278].

While most SRAM-based solutions reported in literature have been used only for flux measurement, it is also possible to measure LET with custom-designed SRAM detectors. A solution presented in [279] uses a custom-designed SRAM-based detector which generates SET pulses in response to particle strikes, and the analog processing circuitry is employed to amplify the pulses and measure their amplitude. Based on measured pulse amplitude, the energy and LET spectra of incident particles can be determined. In this case, all SRAM cells are connected in parallel, so that a particle strike in any cell induces a pulse which can propagate to the output. The solution is designed as a standalone spectrometer and as such is not suitable for the on-chip integration.

3.5.5 3D NAND Flash Detectors

Recently, the use of 3D NAND flash memory with floating gate transistors as a heavy-ion detector has been proposed [280]. Although the detectors based on floating gate transistors have been employed for total dose and dose rate measurement [281, 282], the work [280] is the first to demonstrate the applicability of this concept for detection of energetic particles. The operating principle relies on measurement of the threshold voltage shift of floating gate transistors due to the charge deposited by the incident particles. This allows not only to measure the error rate, but also the particle LET. In addition, due to the 3D structure of NAND memory, the angle of incidence can be estimated. The 3D structure also allows to differentiate between the errors due to energetic particles and those due to electrical noise, as well as to differentiate between single and multi-bit errors (upsets).

Although the 3D NAND flash with floating gate transistors is a promising solution with substantial benefits over other detectors such as SRAM, the main limitation currently is difficulty in integrating it in the target chip. Due to the 3D structure and floating gate technology, this approach may be too complex for integration into a conventional planar CMOS IC designed with standard design tools. In addition, the processing electronics may be complex and costly because it is necessary to measure precisely the change of the threshold voltage of floating gate transistors, which requires the use of analog processing circuitry and analog-to-digital converters.

3.5.6 Comparison of Particle Detectors

Based on previous discussion, a comparison of the analyzed particle detectors, highlighting their strengths and weaknesses, is summarized in Table 3.4. The most widely used particle detectors in space applications are diode-based and SRAM-based detectors. However, none of the existing detectors examined here has optimal performance for the self-adaptive fault-tolerant applications, since each of them has some essential limitations. The limitations of the state-of-the-art semiconductor particle detectors can be sorted into two groups: (i) detectors which can measure both flux and LET are generally costly and require complex (mixed-signal) processing which results in high area and power overheads, (ii) low-cost detectors with low performance overhead cannot measure particle LET, which severely limits their efficiency in real-time SER prediction. In addition, most detectors are to certain extent prone to false alarms, multiple errors or error

accumulation. From the perspective of self-adaptive fault-tolerant applications, an optimal embedded particle detector should provide a trade-off between the accurate measurement of radiation exposure and the low complexity processing logic with low area and power overhead. In addition, the detectors should be suitable for integration with the fault-tolerant systems on the same chip, in order to reduce the overall cost. The lack of such solutions motivates further research on novel low-cost particle detectors suited for monitoring of both particle flux and LET.

Detector type	Advantages	Disadvantages
Bulk built-in current detectors	Provide information on the particle strike location Can be integrated in the target chip	May be prone to false alarms Cannot detect LET variation
Acoustic wave detectors	Provide information on the particle strike location Can be integrated in the target chip	May be prone to false alarms Analog processing increases the overall system complexity Cannot detect LET variation
Diode detectors	Allows for measuring the particle flux, LET and energy spectrum Certain configurations can detect the direction of particle incidence	Analog processing increases the overall system complexity Challenging integration in the same chip with the target system
SRAM detectors	Low cost digital logic required for error detection and correction May be implemented in the same technology as the target circuit	Sensitivity to multi-bit upsets High area and power overhead in standalone implementations Cannot detect LET variation
3D NAND flash detectors	Possibility of measuring the particle flux, LET and angle of incidence	Challenging integration in the same chip with the target system Analog processing increases the overall system complexity

Table 3.4: Comparison of soft error (particle) detectors

3.6 Summary of Open Issues Addressed in this Thesis

With respect to the state-of-the-art outlined in previous discussion, the following are the critical open issues:

 The existing approaches for characterization of SET effects in standard cell libraries based on SPICE simulations are very timing consuming because in most cases it is necessary to conduct a large number of simulations for every gate. Even though this procedure has to be done only once for a given library, it may require a lot of effort due to a large number of standard cells in digital libraries. Besides, the SET database obtained as a result of the characterization is very extensive, composed of look-up tables with a huge number of values (typically in the order of millions). Along with the requirements for memory capacity to store the characterization database, the use of characterization data for subsequent SER analysis may be very time consuming when it is necessary to access a large number of LUTs. <u>Hence, there is a strong need to provide an optimized solution for reducing both the number of simulations during the SET characterization and the total amount of characterization data.</u>

- 2. The standard SET models resulting from the characterization process (critical charge, SET pulse width and SET propagation models) suffer from insufficient accuracy. In most cases, either not all relevant factors are considered or simplified conditions are applied during the model derivation. The use of such models may result in considerable errors in SER evaluation. In addition, the SET models are not fully integrated in the SET characterization process, as there is no a systematic methodology which combines the SET characterization process with the model derivation process. Thus, there is a need for improved SET models which can be integrated into a coherent rad-hard design flow.
- 3. The existing gate-level techniques for hardening the standard combinational cells cannot provide optimal SET mitigation if only a single technique is applied, since each of them produces only a limited improvement of SET robustness, with inevitable performance overheads. In addition, there is no an optimal combination of multiple techniques and there is also no a systematic approach to characterize the gate-level hardening techniques applicable to standard cells. This imposes the need for improved gate-level hardening solutions targeting both the SET generation and the SET propagation, as well as for the overall characterization of different gate-level hardening techniques that will effectively complement the characterization of standard cells.
- 4. The particle detectors employed for soft error monitoring lack some essential features required for dynamic fault tolerance. The main drawback of detectors based on digital readout is the inability to measure the particle LET. On the other side, the detectors which support the LET measurement are characterized by high cost and complexity of processing logic. <u>It is thus necessary to explore new possibilities for the real-time radiation intensity monitoring with low-cost solutions supporting the measuring of both the particle flux and LET.</u>

This work aims to address each of the aforementioned open issues. In such a way, a basis for a costefficient rad-hard design flow could be established. The proposed solutions are presented in detail in the following chapters.

Chapter 4

Characterization and Modeling of SET Effects in Standard Combinational Cells

The information on the SET sensitivity of individual logic cells is essential for efficient and cost-effective SER computation and subsequent selection of the most appropriate SET mitigation measures. To this end, we propose a holistic methodology which addresses the characterization of the standard combinational cells and the respective gate-level SET mitigation configurations. This chapter analyzes the characterization and modeling of SET effects in standard combinational cells, while the gate-level SET mitigation techniques are addressed in Chapter 5. The following discussion is divided into nine sections. Section 4.1 briefly reviews the key challenges of SET characterization in standard cells, and introduces the idea of a holistic characterization methodology. Section 4.2 describes the characterization phases and the setup employed for electrical simulations of SET effects in standard cells. Section 4.3 and Section 4.4 present the simulation analysis of the SET generation and propagation in standard combinational cells, respectively, considering the impact of the most important design, operating and irradiation parameters. In Section 4.5, the general SET-aware design recommendations are proposed based on the characterization results. In Section 4.6, the analytical models for the SET sensitivity metrics (critical charge, SET pulse width and SET propagation) are derived by fitting the simulation results and employing the superposition principle. In Section 4.7, the applicability of the proposed modeling approach to two application-specific cells is analyzed. Section 4.8 describes the SET characterization database, with emphasis on the possibilities for reducing the number of required simulations and the amount of characterization data. Finally, Section 4.9 summarizes the achieved results and outlines the directions for future work.

4.1 Introduction

Any standard technology with sufficient robustness to TID and hard SEEs can serve as a basis for many rad-hard applications, including the space applications. However, because most CMOS technologies are inherently sensitive to soft errors, the RHBD techniques need to be applied in order to achieve the required level of soft error robustness. In that sense, it is required to first evaluate the soft error sensitivity of standard

cells in a given digital cell library. However, due to a number of challenges, the effort that has to be invested in the characterization of complete library, particularly the combinational cells, may be enormous.

Modern digital cell libraries contain hundreds or thousands of combinational cells, typically one order of magnitude more than the sequential cells [65]. The combinational cells exhibit intrinsically differing sensitivity to SETs due to different number, size and arrangement of transistors within each cell. Two cells having the same logic function and size may have different contribution to SET generation and propagation, depending on their position in the target circuit, supply voltage and input levels. Furthermore, a cell may be more vulnerable to direct particle strikes (SET generation) than to SET propagation effects, or vice versa. It is therefore imperative to conduct qualitative and quantitative assessment of both the SET generation and the SET propagation effects for individual cells (gates) in a standard cell library. Because the SETs are analog signals, it is necessary to analyze the electrical response of logic gates in terms of SET generation and propagation sensitivity, considering a wide range of contributing parameters.

As a result of the above mentioned challenges, the characterization of SET effects in a standard cell library is faced with issues related to simulation runtime, size of output database and accuracy of predictive SET models. In addition, the lack of support in commercial design tools for soft error analysis makes the overall characterization process more challenging. To facilitate the integration of soft error analysis into a standard IC design flow, the characterization approach should primarily consider the parameters which are available to the designer and are relevant for the design process. For example, it is sufficient to view the standard cells in terms of their driving strength rather than in terms of transistor sizes, because the sizing is uniform for every standard cell library and is not changed in the design process. Moreover, the technological parameters are often not readily available to the designers, and hence the characterization process may be transparent in terms of technological details.

The characterization results for standard logic gates are employed in the SER analysis to identify the most vulnerable gates in a circuit. Subsequently, appropriate gate-level hardening techniques are applied to a set of the most sensitive gates to reduce the overall SER. However, the selection of the SET mitigation approach is not straightforward due to necessity to comply with the predefined design constraints and the inherent limitations of existing techniques. It may thus be required to perform numerous iterations in the design process until the optimal solution is obtained. For every hardening solution applied to a certain gate in the target circuit, the overall SER has to be re-calculated. This obviously requires further simulation runs, unless there is a pre-characterized database for the hardening configurations.

In order to address the challenges of the standard cell library characterization, and resolve some essential limitations of existing approaches, we introduce a holistic methodology for characterization of SET effects in standard cell library. The idea is to characterize jointly the standard cells and the corresponding gate-level hardening configurations for the standard cells. In that regard, we consider only the hardening techniques that do not require modifying the cell structure. To the best of our knowledge, none of the previous library characterization approaches addresses jointly the standard cells and their hardened configurations. This work aims to establish a flexible characterization and modeling approach than can provide sufficiently transparent interface to the designer while maintaining high accuracy with respect to electrical simulations. Specifically, we aim to: (i) demonstrate the possibility of reducing the number of simulations during the characterization process by exploiting inherent similarities in the SET response, (ii)

establish the analytical models for SET sensitivity metrics based on fitting of simulation results by employing the superposition principle, thus allowing to analyze the individual contribution of each parameter, (iii) introduce a concept of SET sensitivity database by storing the model coefficients in LUTs instead of raw simulation data, thus reducing the amount of output data.

4.2 A Holistic Methodology for Standard Cell Library Characterization

The proposed methodology adopts the SPICE-based simulations for characterization of the SET sensitivity of standard combinational cells. Although the SPICE simulations cannot take into account some relevant physical aspects (e.g. gate/circuit layout, strike location and angle of incidence), they still provide the best trade-off between accuracy and simulation runtime for the analysis of electrical effects of the SET response. In this study, the simulations have been performed with the Cadence Spectre simulator, integrated in the commercial Cadence Virtuoso suite.

In Figure 4.1, the general flow of the proposed methodology is illustrated. The characterization process consists of five main phases:

- (a) Definition of input database,
- (b) Creation of simulation setup for standard cells and corresponding hardened configurations,
- (c) Characterization of SET generation and propagation and establishment of characterization tables,
- (d) Derivation of SET generation and propagation models from the characterization results,
- (e) Formation of SET sensitivity database for standard cells and their hardened configurations.

The input database includes the SPICE (or Spectre) netlists of standard cells and the specification and ranges of input parameters to be analyzed. The netlists of standard cells are integrated in the process design kit (PDK) for a given technology, and can be readily used in circuit simulation tools. As the characterization is done for a particular technology, the details of technological parameters are not taken into account explicitly in simulations, but are rather included implicitly in the standard cell netlists. Thus, the parameters considered in simulations can be grouped into three classes:

- *Design parameters*: Driving strength (size factor) of target gate, driving strength (size factor) of load gate, fan-out (number of load gates), capacitance of interconnections.
- Operating parameters: Supply voltage, temperature, input logic levels.
- *Irradiation parameters*: Linear energy transfer (LET), induced charge, rise and fall time constants of the SET current model.

The main technology chosen for this study is IHP's 130 nm bulk CMOS technology. It is a part of IHP's SiGe BiCMOS technology that has been proven as a viable platform for a wide range of applications, as well as for space missions, and is currently under the European Space Components Coordination (ESCC) evaluation, funded by the European Space Agency (ESA) [283]. Numerous irradiation tests have shown that standard digital cells in investigated technology are tolerant to TID up to 50 krad, and up to 200 krad when the Enclosed Layout Transistors (ELT) are applied [284]. Furthermore, it was shown that standard digital cells exhibit no Single Event Latchup (SEL) up to LET of 67 MeVcm²mg⁻¹ [284]. However, like for

any conventional CMOS technology, the sensitivity of standard digital cells to soft errors due to SETs and SEUs remains as a main design challenge for rad-hard applications. Besides the 130 nm technology, a part of the analysis was done on IHP's 250 nm and UMC's 65 nm technologies. The 65 and 250 nm technologies were used for analysis of two application-specific standard cells: SEL protection switch and Mueller C-element. The two analyzed non-standard cells are specific due to their applicability in the rad-hard solutions, and our objective was to verify the models derived from the characterization results on logic cells which are not common in standard libraries.

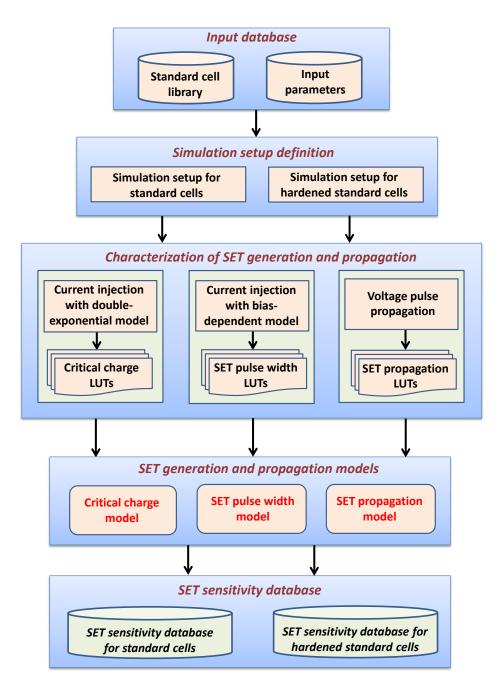


Figure 4.1: Proposed methodology for characterization and modeling of SET effects in standard cells and corresponding hardened configurations

In this study, nine most common types of logic gates have been analyzed: INV, BUF, NAND, AND, NOR, OR, XOR, XNOR, and standard delay cells (SDC). The INV, NAND and NOR are basic (primitive) logic gates which are most frequent in digital designs, and are also used as building blocks of more complex logic gates. The NAND, AND, NOR and OR gates are available in 2-, 3- and 4-input versions, while XOR and XNOR gates are available in 2- and 3-input versions. Thus, the notation NAND2 denotes a 2-input NAND gate, NAND3 is a 3-input NAND gate and NAND4 is a 4-input NAND gate. Similar notation is used for all multi-input gates. The investigated library is also composed of additional complex combinational gates which have not been analyzed in this study, such as MUX, AND-OR, AND-OR-INV, OR-AND and OR-AND-INV. Each type of gate is available in multiple driving strengths. The cells with higher driving strengths are implemented by upsizing the transistors (increasing the channel widths) or connecting more transistors in parallel. The channel width of individual transistors for each driving strength is twice the size of the previous driving strength. For the sake of mathematical modeling, we adopt the notion of size factor S, such that the lowest driving strength x0 has the size factor S = 1, the driving strength x1 has the size factor S = 2, and so on. To differentiate between the target and load gates, the size factor of target and load gates is denoted as S_T and S_L , respectively. Thus, the terms driving strength and size factor will be used interchangeably in the following.

In Table 4.1, the parameters and corresponding simulation conditions (parameter ranges) considered in the characterization process are given. The selected parameters have dominant impact on the SET sensitivity. For each gate, the simulations have been done for all possible combinations of analyzed parameters. However, for the sake of brevity, only the most significant results are presented here. To account for a wide range of possible load settings, the load gates of different type, driving strength and number have been employed. The nominal supply voltage for the analyzed 130 nm technology is 1.2 V, where the minimum possible voltage is 0.8 V (for low power applications) and the maximum permitted voltage is 1.32 V. The nominal temperature is taken as 27 °C, and the considered temperature range is from -40 to 125 °C. The interconnection capacitance is varied from 0 to 10 fC, where the nominal value is 0 fC. For each gate, all possible input levels are considered. The radiation conditions are taken into account through the SET current model defined by timing constants and LET, as will be explained in the following discussion.

It is important to note that the number of parameters affecting the SET generation and propagation is larger than the set given in Table 4.1. The following parameters also define the SET response: (i) transistor's channel length, (ii) ratio between channel width and length of transistors, (iii) ratio between channel width of PMOS and NMOS transistors, and (iv) diffusion constant. The aforementioned parameters may differ from the nominal values due to process variations. Besides, as elaborated in Section 2.6, the SET response is also affected by additional parameters such as layout, aging, and manufacturing defects. However, for the sake of compactness of the analysis, we present here only the analysis for parameters which are essential in the early design phases. The presented analysis is general, and can be easily extended to incorporate other contributing parameters.

For each analyzed logic gate, extensive simulations have been performed to characterize the dependence of three main SET sensitivity metrics (critical charge, generated SET pulse width and propagated SET pulse width) on the selected parameters. A general simulation setup is illustrated in Figure 4.2. To emulate the

particle-induced SETs, a current source was connected successively to all sensitive nodes within the target gate. The sensitive transistors are defined by the input logic levels (off-state transistors are most sensitive), and the critical charge and SET pulse width are analyzed at the output of load gate. To obtain a realistic SET response, a buffer with driving strength x1 is placed between the signal generator and the input(s) of target gate. The same simulation setup is applied for analysis of SET mitigation in Chapter 5.

Parameter	Short notation	Simulation conditions
Driving strength (size factor) of target gate	ST	x0 - x20 (1 - 40) for INV x1 - x20 (1 - 40) for BUF x0 - x4 (1 - 8) for other gates
Driving strength (size factor) of load gate	SL	Same as for target gate
Supply voltage	V _{DD}	0.8 – 1.32 V
Temperature	T _{EMP}	- 40 – 125 °C
Capacitance of interconnections	Cw	$0-10 \ \mathrm{fF}$
Timing parameters of current pulse	$\tau_{RISE} / \tau_{FALL}$	$\begin{array}{l} 10-50 \text{ ps for } \tau_{\text{RISE}} \\ 50-500 \text{ ps for } \tau_{\text{FALL}} \end{array}$
Particle LET	LET	$0.5-60 \text{ MeV cm}^2 \text{mg}^{-1}$
Input logic levels	-	All input level combinations
Input pulse width	T _{IN}	50 – 600 ps

Table 4.1: Parameters analyzed in simulations

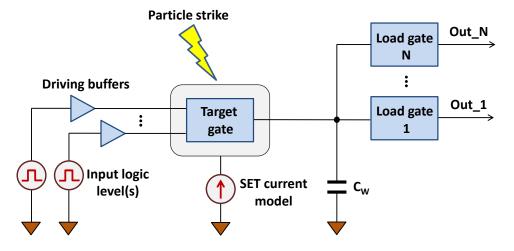


Figure 4.2: Simulation setup for characterization of SET effects in standard cells

For the SET generation analysis, the critical charge and initial SET pulse width have been analyzed. The critical charge was determined as the minimum charge required to cause an SET pulse with amplitude beyond the half of supply voltage at the output of a load gate. The SET pulse width was determined at the level of half of supply voltage. Two current models have been used: the standard double-exponential current

model [187] was used for the critical charge analysis, and the bias-dependent current model [205] for the SET pulse width analysis. Both models were implemented as Verilog-A models. Although the double-exponential current model is not sufficiently accurate in terms of the reproduction of physical mechanisms of SET effects, it still provides acceptable results for the critical charge analysis. However, due to the inherent overdrive effect, the use of double-exponential current model for SET pulse width evaluation is not recommendable. Hence, we have chosen the bias-dependent current model from [205] for the SET pulse width analysis. The LET was varied from 0.5 to 60 MeVcm²mg⁻¹, covering the LET values of most ionizing particles encountered in natural radiation environments such as space. For example, one of the heavy ions with lowest LET is He² (LET = $1.2 \text{ MeVcm}^2\text{mg}^{-1}$), while the most common heavy ion with high LET is Xe¹³¹ (LET = 59 MeVcm²mg⁻¹). The LET value for a particular energetic particle can be obtained from particle-matter simulations with SRIM/TRIM tool.

The selection of current pulses for SET simulations can be done in two ways. One approach is to choose the predefined range of timing parameters for the current pulse based on previous experiments or reports for related technologies. Another approach is to extract a set of current pulses from TCAD simulations for each gate, and apply these pulses in SPICE simulations. While the TCAD simulations provide accurate analysis of SET effects on device level, they are very time consuming, and it would be required to employ a large set of current pulses for each gate in order to cover all possible conditions. Most characterization approaches listed in Table 3.2 have employed the first method – selection of predefined range of current pulse parameters. We have also adopted a similar approach in this work.

For the SET propagation analysis, the trapezoidal voltage pulse was used as a SET model. This model is most commonly used for SET propagation analysis, and it is fairly accurate since the shape of SET pulse becomes very close to trapezoidal after propagation through a single logic gate. The amplitude of the pulse was fixed and only the pulse width was varied. To ease the analysis, the rise and fall time constants were the same, 10 ps. The trapezoidal pulse was fed to the input of each gate, while other inputs (if any) were set to the logic levels which enable the pulse propagation. As the propagation effects are related to the circuit structure and are not dependent on radiation conditions, no radiation-related parameters were considered in this case. However, the results from the analysis of generated SET pulse width have been used for selection of appropriate ranges for the trapezoidal pulse width.

The simulation results for each gate are stored in respective two-dimensional (2D) LUTs, where each LUT represents the variation of one SET metric in terms of two parameters, for nominal values of all other contributing parameters. As elaborated in Section 3.2, the state-of-the-art approach is to store the raw simulation data in LUTs and use this for subsequent SET analysis in a combinational circuit. However, this requires large memory capacity to store a huge amount of characterization data, and significant time is needed to access and read the LUTs during the SET analysis. To reduce the amount of characterization data and thus simplify the SET analysis, the analytical models for the SET critical charge, generated SET pulse width and propagated SET pulses width are established from the simulation data. Then, storing only the model (fitting) parameters in the LUTs gives a SET generation database with reduced memory requirements. In addition, proposed approach allows for reducing the runtime for the SET analysis of a given circuit because less time is required to read several model parameters and compute the corresponding SET sensitivity metrics, than to search a large number of LUTs.

4.3 SET Generation Analysis

This section investigates the dependence of SET generation metrics (critical charge, nominal SER and initial SET pulse width) on the parameters listed in Table 4.1. A detailed characterization of all selected standard cells has been performed to quantify the change of the critical charge and SET pulse width for all combinations of investigated parameters.

4.3.1 Critical Charge Analysis

As elaborated in Section 2.4 and 2.6, the critical charge is a key metric for assessing the vulnerability of individual logic gates to particle strikes. Thus, it can be used as a figure of merit for comparing the SET sensitivity of different gates. In general, smaller gates are most vulnerable to particle strikes. However, due to the changing operating and radiation conditions, the value of critical charge of any circuit node may vary continuously, potentially resulting in significant SER variations.

4.3.1.1 Critical Charge of Single-Input Logic Gates

The two most widely used single-input logic gates are INV and BUF. Because of their simple design, a particle strike in a sensitive transistor can easily result in an observable SET at the gate's output. As BUF is composed of two cascaded inverters with different driving strengths, only the results for INV will be presented.

In Figure 4.3, the critical charge of inverter as a function of its size factor, for different sizes of load inverter, both input levels and nominal values of all other parameters, is illustrated. It can be seen that the relation between critical charge and inverter's size factor exhibits good linearity for size factors up to S_T = 8. By increasing the size of inverter, both the node capacitance and the driving current are increased, enabling faster dissipation of induced charge, and resulting in proportional increase of the critical charge. However, this dependence deviates from linearity for size factors greater than 8. For low input level, the dependence is slightly supra-linear, while for high input it is sub-linear. Such behavior has not been reported in previous works where the analyzed size factors were usually smaller than 8. We assume that the observed non-linearity is due to the reduced driving current when the gate size is increased beyond certain threshold, but further research has to be conducted to investigate this effect.

The critical charge also increases linearly with the increase of the size factor of load gate. However, the impact of load size is significantly weaker compared to that of the target gate. For example, according to the obtained results, the critical charge may increase by 100 % when the size factor of target gate is increased from 1 to 2, but only up to 15 % when the size factor of load gate is increased from 1 to 4. That is because the increase of the target gate's size increases both the drive current and the node capacitance, while larger load gate increases only the node capacitance. Though, it is important to mention that the quantitative impact of load gate also depends on the driving strength of the target gate. A larger load gate will have more significant contribution in the critical charge if the target gate is small.

In general, the logic gates in a combinational circuit may have multiple load gates (fan-out > 1) as depicted in Figure 4.2, and one type of gate can be loaded by any other type of gate. Each additional load gate contributes to the increase of the critical charge, i.e., a gate driving multiple gates will be more robust to particle strikes than a gate driving only one gate. To investigate the impact of different load settings, the

simulations have been conducted with various combinations of load gates. The critical charge values for inverter with driving strengths x1, x2 and x4, for low input level and eight different load gates, are given in Table 4.2. It can be seen that each type of load gate produces different quantitative impact on the critical charge. This difference is due to the fact that the critical charge is determined at the output of load gate. Interestingly, the difference between the critical charge values for two load gates increases with the increase of the size of target gate. Similar trend was observed for high input level. When load consists of multiple gates, the critical charge of the target node will increase proportionally to the total input capacitance of load gates. Note that the input capacitances of all gates are available in the standard cell library characterization file (.LIB file) which is a part of PDK.

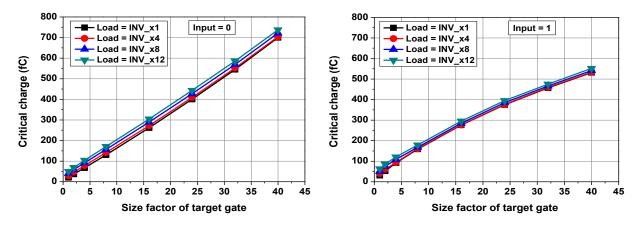


Figure 4.3: Critical charge of inverter as a function of its size factor, for different load sizes and both input levels, and for nominal supply voltage (1.2 V) and temperature (27 °C)

Lood gata	Qcrit (fC) for INV gate			Load gata	Qcrit (fC) for INV gate		V gate
Load gate	INV_x1	INV_x2	INV_x4	Load gate	INV_x1	INV_x2	INV_x4
INV_x1	36.6	67.2	136.8	AND2_x1	40.3	78.6	158.9
NAND2_x1	38.3	70.3	141.7	OR2_x1	43.8	84.8	174.4
NOR2_x1	39.3	72.3	146.9	XNOR2_x1	45.9	83.8	162.1
BUF_x1	40.3	77.2	157.9	XOR2_x1	47.2	86.9	171.4

Table 4.2: Critical charge for INV gate with driving strengths x1, x2 and x4, for various loadconfigurations and low input level

Another important contributor to the critical charge is the capacitance of interconnections. The simulation results have shown that the critical charge increases roughly by 1 fC per 1 fF of the interconnection capacitance. In a practical circuit the capacitance of interconnections may be in the order of several fF, depending on the wire length, and this information can be obtained from the post-layout parasitic extraction. Therefore, the contribution of capacitance of interconnections may be remarkable in the case of logic gates with low critical charge. For example, for a gate with nominal critical charge of 20 fC, the interconnection capacitance of 2 fF will cause a 10 % increase of critical charge. The dependence of critical charge on supply voltage, for low input level and different drive strengths of target and load gates, is depicted in Figure 4.4. For clarity, the supply voltage is expressed as the change with respect to nominal value (1.2 V). As the supply voltage increases, the transistors' driving current also increases, enabling faster dissipation of induced charge. By increasing the supply voltage for 0.1 V, the critical charge increases by approximately 10 %, while the reduction of supply voltage by 0.4 V (from 1.2 to 0.8 V) decreases the critical charge by around 30 %.

It can be seen in Figure 4.4 (a) that the absolute change of critical charge for a given driving strength of target gate is almost the same for equal positive and negative increments of supply voltage with respect to the nominal value. For example, for INV_x1 as a target gate, the critical charge increases by 8 fC when the supply voltage is increased from 1.2 to 1.32 V, and decreases by 8 fC when the supply voltage is decreased from 1.2 to 1.08 V. The dependence of critical charge on supply voltage is linear from 1 to 1.32 V, but is slightly nonlinear in the range from 0.8 to 1 V. By increasing the driving strength of target gate, the slope of the relation between critical charge and supply voltage, as depicted in Figure 4.4 (b). However, the impact of load may be more pronounced if other types of load gates are used (e.g., XOR and XNOR), and thus it is important to consider also the impact of load.

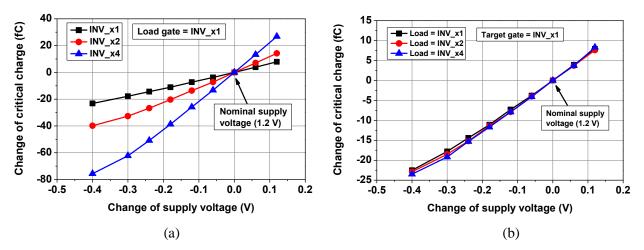


Figure 4.4: Change of critical charge of INV gate as a function of the change of supply voltage, for: (a) different driving strengths of target inverter, (b) different driving strengths of load inverter

The effect of temperature on the critical charge is shown in Figure 4.5. All temperature values have been normalized by subtracting the nominal value (27 °C). The temperature has opposite effect to that of supply voltage. Namely, a temperature increase leads to a decrease of transistors' driving current. Consequently, the transistor's ability to dissipate the induced charge is reduced at elevated temperatures, resulting in lower critical charge. In quantitative terms, the impact of temperature is weaker than that of supply voltage, accounting for approximately 10 % of the change of critical charge over the range from -40 to 125°C. The relation between critical charge and temperature slightly deviates from linearity, and the non-linearity gradually increases with the size of target gate. The variation of load size and supply voltage produce a minor impact on the relation between critical charge and temperature, and for this reason have not been shown here.

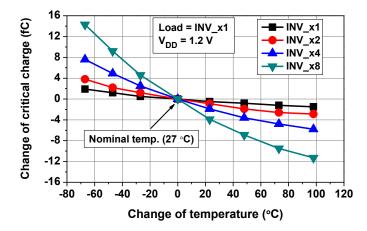


Figure 4.5: Change of critical charge of INV gate as a function of the change of temperature with respect to $T_{EMP} = 27$ °C, for different driving strengths of INV gate and low input level

The change of critical charge of an inverter in terms of the rise and fall time constants of injected current pulse is illustrated in Figure 4.6. The simulations have been done by varying one time constant, while the other is kept at a fixed value. In both cases the critical charge is almost a linear function of time constants. The fall time constant has stronger impact and causes an increase of critical charge by several times, while the rise time constant causes an increase of critical charge by a maximum of 30 %. Note that the time constants depict the charge collection process in the device. Thus, the increase of critical charge with the time constants can be explained by the fact that wider current pulses imply that the charge collection process takes longer time, which means that more charge has to be induced to alter the logic level. The slope of the dependence between critical charge and time constants of the current pulse increases with the size of target gate, but is less dependent on other investigated parameters.

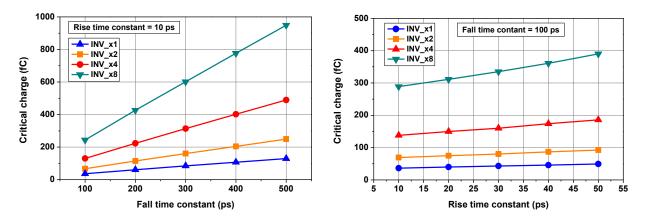


Figure 4.6: Critical charge of INV gate as a function of rise and fall time constants of the current pulse, for different driving strengths of INV gate and low input level

4.3.1.2 Critical Charge of Multiple-Input Logic Gates

Figure 4.7 depicts the critical charge of the output nodes of six two-input gates as a function of size factor and input levels, while all other parameters are at nominal values. In all cases the critical charge increases

almost linearly with the size factor. As the investigated 2-input logic gates are available in size factors up to 8, no degradation of linearity like for INV was observed. For some input levels the critical charge is almost identical, due to the equivalence of the resistance of on-state transistor networks within the gates. For AND2 and OR2 gates, three input levels give the same critical charge because the output node is inverter, and hence for three input levels the output will be at the same level. The slope of the relation between critical charge and size factor is larger for NAND gate with 00 input and for NOR gate with 11 input than for other input levels. That is because, for these two inputs, the two parallel transistors in NAND2 and NOR2 gates are in on-state, providing two conductive paths for dissipation of the induced charge. The dependence on other analyzed parameters (supply voltage, load size, capacitance of interconnections, temperature, and timing constants of the injected current pulse) is qualitatively similar as for INV, and the quantitative variations are also within the ranges reported in previous section.

The results in Figure 4.7 show that the difference between the critical charge values for different input levels increases with the driving strength. In addition, the critical charge for certain input level and higher driving strength may be similar or lower than the critical charge for another input level and lower driving strength. For example, in the case of NAND2 gate, the critical charge of output node for input 00 and size factor 4 is almost the same as for other input levels and size factor 8. These observations indicate that the traditional view of larger gates as being by default more robust to SETs may not be valid under all possible operating conditions, and hence the mutual impact of gate size factor and input levels must be considered in SET robustness evaluation.

In the case of 3- and 4-input gates, the critical charge values can be sorted into several groups, where each group consists of several input levels for which the critical charge is almost the same. This is shown for NAND3, AND3, NAND4 and AND4 gates in Tables 4.3 – 4.6, respectively. Similar behavior was observed for other 3- and 4-input gates. The rows shaded with the same color indicate the input levels for which the critical charge values are almost the same. For example, for NAND3 gate the critical charge can be classified into four groups, while for NAND4 gate five groups can be identified. Note that the critical charge values are almost the same for input levels with the same number of zeros or ones, and similar trend was noticed for NOR3 and NOR4 gates (not shown here). This can be explained by the fact that, due to the symmetry of these gates, the equivalent resistance will be almost identical for input levels with the same number of on/off transistors. On the other hand, for AND3 and AND4 gates the situation is somehow different, with only two critical charge groups. This is related to the fact that the critical charge was analyzed for the output node of each gate. Since AND gate has an inverter in the output stage, only two different sensitivity levels for the output node are possible. For the NAND section of AND gate, the trend is similar as shown in Table 4.3 and Table 4.5.

An important observation is that there is no a clear dependence between the SET sensitivity and the number of input pins. As can be seen in Tables 4.3 and 4.5, for low level at all inputs, the critical charge of NAND3 is lower than that of NAND4, while the situation is opposite for high level at all inputs, i.e., the critical charge of NAND3 is higher than that of NAND4. Similar trend was noticed for other gates. Such a trend is attributed to the difference in gate structure. Namely, certain gates have such transistor arrangement that increasing the number of pins increases the equivalent resistance, which results in lower driving current and therefore lower critical charge.

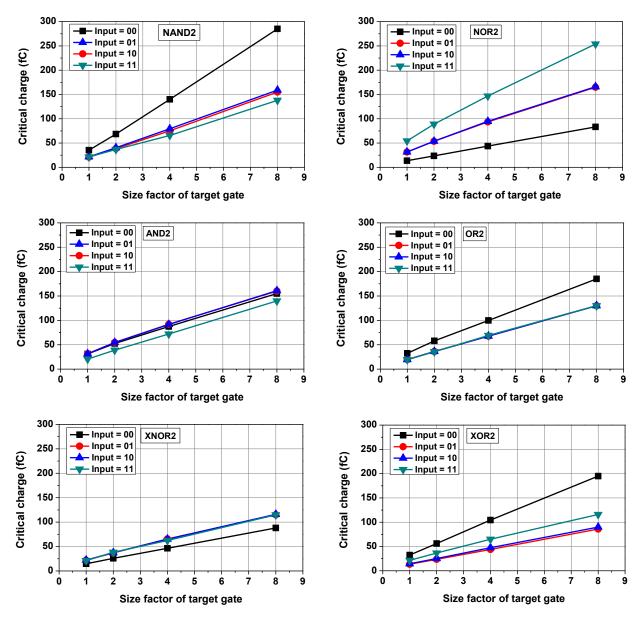


Figure 4.7: Critical charge of two-input logic gates as a function of their driving strength and input levels, while all other parameters are at nominal values

Based on the presented results, the number of simulation runs for characterization of the SET robustness of 3- and 4-input gates can be significantly reduced since it would not be necessary to repeat the simulations for input levels that have similar critical charges. As the observed trend is related to the gate structure and sizing, similar approach for reducing the number of simulations can be applied to a standard cell library designed in a different technology. More details on the use of inherent similarities in the SET response for reducing the number of characterization simulations is given in Section 4.8.1.

It is worth mentioning that all presented results are for the output nodes of respective logic gates (current is injected in the gates' output). The same analysis was done for all internal nodes of multi-input gates. Due to qualitatively similar dependencies, the results have not been shown here. For example, for AND and OR gates, the critical charge values of internal nodes are similar to those for NAND and NOR gates. However,

it is important to note that for certain gates such and XOR and NOR, some internal nodes are more sensitive than the output node. For this reason, it is crucial to take into account the sensitivity of all nodes. In addition, it is important to state that certain input nodes in some gates are not sensitive even if they are in off-state, because of the lack of conductive path to the output. This depends merely on the gate structure and such nodes can be identified by analysis of the gate topology.

Input	Qcrit (fC)			
	x0	x1	x2	
000	61	111	220	
001	46.2	81.2	153.3	
010	46.3	80.3	152.8	
011	30	49.3	87.5	
100	46.9	82.4	154.6	
101	31	50.3	90.3	
110	31	50.3	89.8	
111	26.9	39.3	63.4	

Table 4.3: Q_{CRIT} for output node of NAND3

Table 4.5: Q_{CRIT} for output node of NAND4

Input		Qcrit (fC)				
	x0	x1	x2			
0000	69.3	136	279.3			
0001	54.7	105	211.7			
0010	54.7	104.7	212			
0011	40.5	73.7	147.4			
0100	54.7	104.7	212			
0101	40.2	73.7	146.9			
0110	40.1	73.7	146.8			
0111	24.7	43.2	82.1			
1000	55.7	106.8	212.8			
1001	41.2	75.8	150.5			
1010	41.1	76.2	150.5			
1011	25.7	45.7	85.7			
1100	40.5	75.8	150.5			
1101	25.8	45.8	84.7			
1110	25.7	45.2	84.7			
1111	18.9	30	51.6			

Table 4.4: QCRIT for output node of AND3

Input	Qcrit (fC)			
	x0	x1	x2	
000	41.6	62.6	97.9	
001	41.6	63.7	98.9	
010	41.6	63.6	98.9	
011	41.5	64.7	102.4	
100	41.6	63.7	98.9	
101	41.5	64.7	102.1	
110	41.6	64.7	102.6	
111	30	49.4	82.6	

Table 4.6: Q_{CRIT} for output node of AND4

Input		Qcrit (fC)				
	x0	x1	x2			
0000	34.5	55.7	92.5			
0001	34.5	55.8	91.5			
0010	34.7	55.8	91.5			
0011	34.7	56.3	92.4			
0100	34.7	56.3	92.4			
0101	34.6	55.8	92.4			
0110	34.6	55.8	92.4			
0111	34.7	56.3	92.4			
1000	34.7	56.4	92.4			
1001	34.7	56.3	92.6			
1010	34.7	56.3	92.6			
1011	34.7	57.9	92.4			
1100	34.7	55.8	92.4			
1101	34.7	56.3	95.7			
1110	34.7	57.8	95.7			
1111	24.2	43.5	77.8			

4.3.2 Nominal Gate-Level SER

In previous discussion, the qualitative and quantitative dependence of critical charge on the most important contributing parameters has been analyzed. The simulation results have shown that the size of target gate, input logic levels and timing parameters of the current pulse have strongest impact on critical charge,

whereas the impact of supply voltage, temperature, load size and capacitance of interconnections is moderate. Based on the critical charge values for given settings and the sensitive area of each node in a gate, the nominal SER per gate, as the overall measure of the SET generation sensitivity, can be calculated. Thus, in this section, the SET generation sensitivity of investigated gates is compared in terms of nominal SER. As the critical charge varies with the input levels, the sensitive area will vary accordingly. It is important to note that although the gates with higher driving strength have larger size, due to optimized layout the gate size does not increase twice by doubling the driving strength. The sensitive area (drain area of transistors in off-state) for each gate is determined from the cell layout. Note that PMOS transistors have larger sensitive area because their overall area is larger.

To determine the nominal SER of each gate, we have applied the model of Hazucha and Svensson, defined by the relation (2.3) (see Section 2.4.3). According to this model, the SER of a node is defined as a function of particle flux F, sensitive area of node A, critical charge of node Q_{CRIT} and charge collection efficiency Q_S . The nominal SER for a given input logic level is determined as the sum of SER values for all sensitive nodes (transistors). As the dependence between SER and flux F is linear, for the sake of simplicity we have taken the unity value of flux (F = 1). The sensitive area is taken as the drain area. By interpolating the results from [103], the charge collection efficiency Q_S for 130 nm technology is approximately 17 fC for NMOS transistor, and 8 fC for PMOS transistor. This difference comes from the fact that the collection depth of PMOS transistor is smaller than that of NMOS transistor, and hence PMOS transistor can collect less charge. Note that Q_S is defined by the doping profile and supply voltage. For a given technology the doping profile is fixed, and therefore its impact on Q_S is not relevant for SER analysis. According to [285], it can be assumed that the dependence of Q_S on supply voltage is negligible, and thus the supply voltage influences the SER only through Q_{CRIT} .

In Table 4.7, the SER values for INV_x1 gate, for both input levels and corner values of supply voltage and temperature, are given. For comparison, the absolute and normalized SER values are shown. The normalization was done by dividing with the SER value for nominal conditions (1.2 V, 27 °C). As can be observed, the SER is higher for low input level (when NMOS is sensitive). This is the result of lower critical charge for low input level and higher charge collection efficiency of NMOS transistor. However, the variation of SER is more pronounced for high input level. This is mainly due to the fact that the charge collection efficiency of PMOS transistor, which is sensitive for high input level, is more than twice lower than that of NMOS transistor. As a result, the change of Q_{CRIT}/Q_S term in relation (2.3) will be larger for high input level. In addition, two important trends can be noticed. First, the SER may change by more than two orders of magnitude when input levels change. Second, the SER may vary by more than 50 % under different supply voltage and temperature corners. Although supply voltage and temperature have moderate impact on critical charge, as previously demonstrated, a minor change in either supply voltage or temperature leads to exponential increase of SER in accordance with relation (2.3). It is important to note that the combination of low supply voltage and high temperature may increase the SER by more than 5 times.

The nominal SER values for all investigated gates, for all input levels and driving strengths x1 and x2, are given in Table 4.8. For each gate type, the maximum SER is shown in red. The trend observed for INV, i.e., variation of SER by at least one order of magnitude as input levels are changed, is also typical for other gates. It is particularly interesting to compare the NAND2 and NOR2 gates as they can be used to implement

any logic function. If the average SER for all input levels is calculated, the NOR2 gate will have higher SER than NAND2, and thus it can be said that NAND2 gate is more favorable choice for the design of robust circuits. Furthermore, it can be seen that NOR2 gate has higher SER than all other gates for 00 input, and it may vary by four orders of magnitude as a result of the change of input logic levels, which is the largest SER variation for the investigated cells. Concerning the average SER for all input levels, the complex gates have higher average SER than the basic ones because of larger number of sensitive nodes and thus larger total sensitive area. Among the investigated gates, the XNOR2 and XOR2 gates have the highest average SER. By increasing the driving strength from x1 to x2, the SER of most gates drops roughly by one order of magnitude. This is due to the fact that the increase of driving strength may double the critical charge, whereas the sensitive area increases less than 50 % from driving strength x1 to x2.

Operating conditions	Nominal SER (FIT)			
Operating conditions (supply voltage, temperature)	Input = 0		Input = 1	
(Supply voluge, temperature)	Absolute	Normalized	Absolute	Normalized
1.2 V, 27 °C	2.47×10-5	1	4.32×10 ⁻⁷	1
1.32 V, 27 °C	1.66×10-5	0.66	1.09×10 ⁻⁷	0.25
1.32 V, -40 °C	1.38×10-5	0.55	5.99×10 ⁻⁸	0.14
1.08 V, 27 °C	3.63×10 ⁻⁵	1.45	1.50×10 ⁻⁶	3.47
1.08 V, 125 °C	3.85×10 ⁻⁵	1.54	2.30×10 ⁻⁶	5.32

Table 4.7: Nominal SER for INV_x1, for corner values for supply voltage and temperature

Table 4.8: Nominal SER for logic gates with driving strengths	x1 and x2 ($V_{DD} = 1.2 \text{ V}, T_{EMP} = 27 ^{\circ}\text{C}$)
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Gate type	Nominal S	SER (FIT)	Gate typeNominal SER (F(input levels)Size x1	SER (FIT)	
(input levels)	Size x1	Size x2		Size x1	Size x2
INV (0)	2.47×10-5	5.00×10 ⁻⁶	BUF (0)	2.81×10-5	2.47×10 ⁻⁵
INV (1)	4.32×10 ⁻⁷	4.16×10 ⁻⁹	BUF (1)	2.72×10 ⁻⁵	5.40×10 ⁻⁶
NAND2 (00)	2.70×10 ⁻⁶	5.90×10 ⁻⁸	AND2 (00)	3.13×10 ⁻⁶	6.32×10 ⁻⁸
NAND2 (01)	1.60×10 ⁻⁵	2.67×10-6	AND2 (01)	1.64×10 ⁻⁵	2.67×10 ⁻⁶
NAND2 (10)	2.98×10 ⁻⁵	4.27×10 ⁻⁶	AND2 (10)	3.02×10 ⁻⁵	4.27×10 ⁻⁶
NAND2 (11)	3.55×10 ⁻⁶	1.89×10 ⁻⁷	AND2 (11)	2.83×10 ⁻⁵	5.20×10 ⁻⁶
NOR2 (00)	7.09×10 ⁻⁵	3.42×10 ⁻⁵	OR2 (00)	7.13×10 ⁻⁵	3.42×10 ⁻⁵
NOR2 (01)	2.69×10 ⁻⁷	2.88×10-9	OR2 (01)	2.50×10-5	5.00×10 ⁻⁶
NOR2 (10)	6.22×10 ⁻⁶	8.50×10-7	OR2 (10)	3.10×10 ⁻⁵	5.85×10-6
NOR2 (11)	6.60×10 ⁻⁹	7.27×10 ⁻¹²	OR2 (11)	2.47×10 ⁻⁵	5.00×10 ⁻⁶
XNOR2 (00)	3.34×10 ⁻⁵	1.44×10 ⁻⁵	XOR2 (00)	7.59×10 ⁻⁵	5.91×10 ⁻⁵
XNOR2 (01)	1.24×10 ⁻⁵	9.20×10 ⁻⁶	XOR2 (01)	3.55×10-5	1.68×10 ⁻⁵
XNOR2 (10)	2.24×10 ⁻⁵	1.70×10 ⁻⁵	XOR2 (10)	3.69×10 ⁻⁵	1.73×10 ⁻⁵
XNOR2 (11)	1.73×10 ⁻⁵	2.18×10 ⁻⁶	XOR2 (11)	4.56×10 ⁻⁵	2.00×10 ⁻⁷

4.3.3 SET Pulse Width Analysis

The width of the SET pulse generated at the output of a logic gate is crucial for determining the electrical and temporal masking factors, i.e., for the subsequent SET propagation analysis. In this section, we analyze the impact of most important design, operating and irradiation parameters on the qualitative and quantitative variation of the SET pulse width.

4.3.3.1 SET Pulse Width in Single-Input Logic Gates

Analogously to the critical charge, the SET pulse width obtained from SPICE simulations strongly depends on the rise and fall time constants of the injected current pulse, whereas the fall time constant has more dominant impact. It should be recalled that the SET pulse width under real irradiation will vary even for constant LET, due to random strike locations. As a result, a distribution of SET pulse widths is obtained for a given LET. Thus, we have conducted the simulations for the rise time constants from 10 to 50 ps, and the fall time constants from 50 to 500 ps. These ranges cover the typical SET pulse widths that can be induced in the investigated technology. Without loss of generality, here are presented only the results for the rise and fall time constants of 10 and 100 ps, respectively. These values have been chosen because of very good agreement with the experimental results for 130 nm technology reported by Narasimhan *et al.* [115].

For comparison, the simulation results for IHP's INV_x1 gate and a sample of experimental results for inverter chain from [115] are depicted in Figure 4.8. The simulation results in Figure 4.8 (a) illustrate the SET pulse width as a function of fall time constant, for the rise time constant of 10 ps and LET values of 10, 30 and 60 MeVcm²mg⁻¹. As can be noticed, the SET pulse width increases with the increase of the fall time constant, and the difference between the SET pulse widths for different LETs becomes larger as fall time constant increases. Note that for the fall time constant of 100 ps, the simulation results give the pulse widths of 380 ps, 480 ps and 590 ps, for the three investigated LET values, respectively. On the other hand, as demonstrated by Narasimhan *et al.* [115], the experimentally measured average SET pulse widths for inverter chain are around 300 ps, 500 ps and 600 ps, for the three aforementioned LET values. This confirms that the chosen timing constants (10 / 100 ps) mimic very well the real SET pulses.

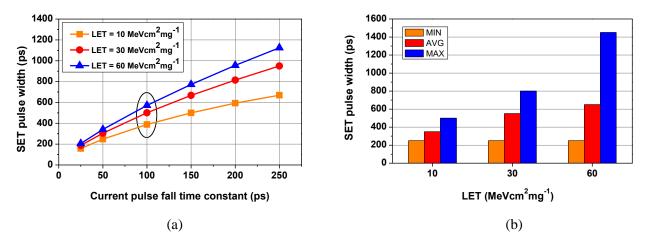


Figure 4.8: SET pulse width for LET of 10, 30 and 60 MeVcm²mg⁻¹: (a) SPICE simulation results for INV_x1 gate, (b) minimum, average and maximum values measured by Narasimhan *et al.* [115]

In Figure 4.9, the SET pulse amplitude and width at the output of INV_x1 gate as a function of LET are illustrated. The results have been obtained from simulations with the nominal supply voltage of 1.2 V and temperature of 27 °C, with INV_x1 as a load. For LET values above the threshold LET, the SET pulse amplitude increases rapidly and reaches the maximum amplitude (supply voltage level) at LET below 1.2 MeVcm²mg⁻¹. As most energetic particles have LET greater than 1 MeVcm²mg⁻¹, it can be expected that in most cases the full-swing SET pulses would be induced. However, the SET pulses with lower amplitudes

could occur in logic gates with higher driving strengths, but it is sufficient to consider the SETs with maximum amplitude as this is the most critical case. Similarly, the SET pulse width increases rapidly up to the LET of around 10 MeVcm²mg⁻¹, and then continues to increase monotonically as LET increases. This is in good agreement with the previous results from SPICE and TCAD simulations [115]. The rate of increase of SET pulse width at higher LET values is reduced because the amount of deposited charge is limited by the charge collection volume of the transistor. For low input level, the SET pulse is approximately 50 ps wider than for high input level. This is in accordance with the fact that the threshold LET (or critical charge) for low input is lower than for high input, i.e., an off-state NMOS transistor is more sensitive to particle strikes than an off-state PMOS transistor.

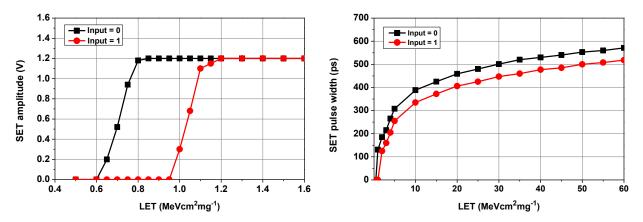


Figure 4.9: SET pulse amplitude and width as a function of LET, for current injection in INV_x1

Figure 4.10 (a) illustrates the SET pulse width as a function of LET, for different driving strengths of target inverter and a single INV_x1 load gate. The SET pulse width decreases by 60 - 90 ps for every increment of driving strength. At the maximum driving strength x20 and LET = $60 \text{ MeV cm}^2\text{mg}^{-1}$, the SET pulse width is reduced by around 50 % compared to that for the driving strength x1. This is because the gates with higher driving strength have larger node capacitance and driving current, allowing faster dissipation of the particle-induced charge. An important observation, that will be essential for constructing the SET pulse width model in Section 4.6.2, is the proportionality between the SET pulse width decrease and the gate size. It should be noted that the threshold LET for each driving strength can be calculated from the previously obtained critical charge values by using the relation (2.2) (see Section 2.4). Thus, it is not necessary to repeat the simulations to determine the threshold LET during the SET pulse width analysis.

The dependence of SET pulse width at the output of INV_x1 gate on the driving strength of a load inverter, for low input level, is illustrated in Figure 4.10 (b). Two regions can be identified when the x-axis is presented in log-scale: (i) a region of low LET where the increase of load size results in a decrease of SET pulse width, and (ii) a region of higher LET where the increase of load size leads to an increase of SET pulse width. The boundary between the two regions is at fixed value of LET, beyond which the induced current is higher than the driving current of the target gate. We denote this boundary as LET_{DRIVE}, as it will be essential parameter for SET pulse width model derivation in Section 4.6.2. Although the increase of load size results in moderate increase of threshold LET, if the deposited charge is significantly higher than the threshold level, the load will have opposite effect on the pulse width, i.e. the SET pulse width will increase

for larger loads. In other words, as can be seen in Figure 4.10 (b), the generated SET pulse width increases for higher LET and larger load. This effect was observed in a previous study [128], and it is attributed to the fact that increasing the load size results in higher node capacitance. As a consequence, longer time is required to charge and discharge the capacitance, thus resulting in longer SETs. It can be expected that the SET pulse width will eventually begin to decrease at certain large size of the load gate, as demonstrated in [128]. However, this occurs for high driving strengths which are not available for most standard logic gates, as most gates have driving strength below x8. It is though important to note that the impact of load is also related to the size of the target gate. If the target gate has larger driving strength than the load gate, the impact of load on the SET broadening will be weaker. Similar effect was observed for other types of load gates as well as for multiple load gates (fanout > 1).

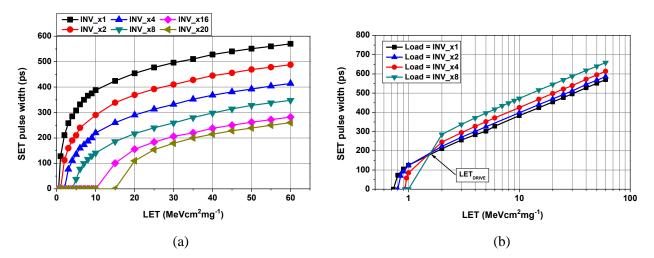


Figure 4.10: SET pulse width as a function of LET: (a) for different driving strengths of target inverter with low input level and INV_x1 as a load gate, and (b) for INV_x1 as a target gate with low input level and different driving strengths of load inverter

Besides the individual impact of the driving strength of target and load gates, it is important to consider their combined impact as well as the impact of multiple load gates. The change of generated SET pulse width for different driving strengths of target inverter and different load settings, is illustrated in Figure 4.11. As a result of increase of either the driving strength of a single load inverter or the number of load inverters, the SET pulse width increases linearly, and these dependences can be well fitted to linear functions, with correlation coefficient $R^2 > 0.98$. The change of the driving strength of a single load inverter from x1 to x8 produces similar effect as the increase of the number of INV_x1 load inverters from 1 to 6. However, the impact of load size is weaker for larger target gates, and this is reflected in smaller change of SET pulse width, as depicted in Figure 4.11. In other words, the slope of the linear function which expresses the change of SET pulse width in terms of load size decreases roughly linearly with the driving strength of target inverter. Similar trend was observed for other types of load gates.

Figure 4.12 (a) depicts the SET pulse width in terms of LET and V_{DD} , for INV_x1 as a target gate, low input level and INV_x1 as a load gate. By increasing V_{DD} , the SET pulse width decreases. This is related to the fact that higher supply voltage increases the driving current in the target gate, thus allowing faster dissipation of induced charge, i.e., the gate will restore the normal state faster if the driving current of the

on-state transistor is higher than the particle-induced current. An important observation is that the change of SET pulse width is almost the same for identical increase and decrease of supply voltage. For example, by increasing the supply voltage for 0.12 V above the nominal value (from 1.2 to 1.32 V), the SET pulse width decreases by approximately 30 ps at LET = 60 MeVcm²mg⁻¹. Similarly, when the supply voltage decreases by 0.12 V, the SET pulse width increases by 30 ps for the same LET. The variation of the SET pulse width is uniform across the investigated LET range.

The temperature effect on SET pulse width, for INV_x1 as a target gate, high input level and INV_x1 as a load gate, is illustrated in Figure 4.12 (b). As the temperature is increased from -40 to 125 °C, the SET pulse width increases by 18 ps, for LET from 1 to 60 MeVcm²mg⁻¹. This change accounts for 3 - 15 % variation of the SET pulse width, whereby the largest impact of temperature is for LET < 5 MeVcm²mg⁻¹. The change of SET pulse width from -40 to 27 °C is almost equal to the change from 27 to 125 °C. For low input level, the impact of temperature is weaker, causing a maximum of \pm 10 ps variation of SET pulse width over the investigated temperature range. The difference between the response for low and high input levels is due to different impact of temperature on PMOS and NMOS transistors.

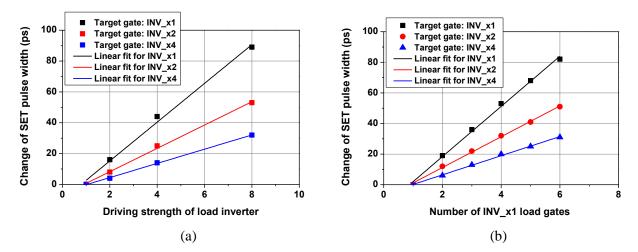


Figure 4.11: SET pulse width for LET = $60 \text{ MeV cm}^2\text{mg}^{-1}$, as a function of: (a) driving strengths of target inverter and load inverter, and (b) driving strength of target inverter and number of INV_x1 load gates

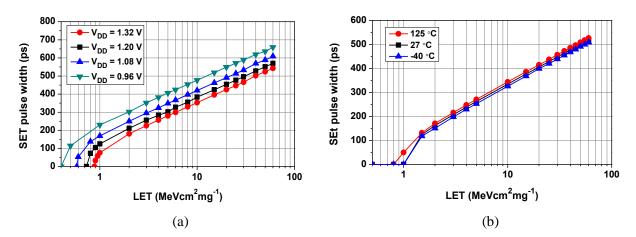


Figure 4.12: SET pulse width at the output of INV_x1 gate, as a function of LET and: (a) supply voltage, and (b) temperature

4.3.3.2 SET Pulse Width in Multiple-Input Logic Gates

In qualitative terms, the dependence of SET pulse width in 2-, 3- and 4-input logic gates on the analyzed parameters is similar as for single-input gates. In Figure 4.13, the SET pulse width as a function of LET, for NAND2_x1 and NOR2_x1 gates, is illustrated. The SET pulse width for different input levels corresponds well to the results obtained for critical charge, i.e., gates with lower critical charge generate longer SET pulses. For NAND2 gate, the worst-case (longest) SET pulse width is obtained for 01, 10 and 11 inputs. Note that the lowest critical charge for NAND2 gate is for 11 input, but the results for 01 and 10 input levels are very close to that for 11 input. On the other side, the most sensitive input for NOR2 gate is 00, with the pulse width at least 150 ps longer than for other inputs. These results agree well with the observation of Limbrick *et al.* [126] that the worst-case pulse widths are obtained when at least one input is at low (0) level. By increasing the drive strength from x1 to x2, the SET pulse width will decrease by 50 – 80 ps over the investigated LET range. The guantitative impact of the size of load gates, and temperature variations, is similar as for 1-input gates. The supply voltage variation produces slightly larger change of SET pulse width decreases/increases by approximately 40 ps.

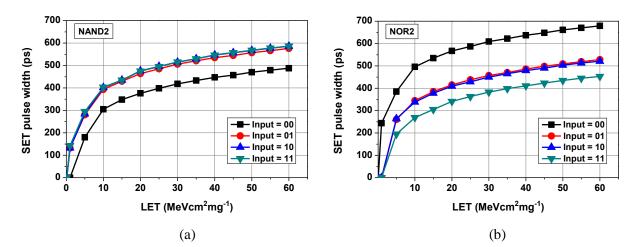


Figure 4.13: SET pulse width as a function of LET, for: (a) NAND2_x1, and (b) NOR2_x1

4.3.3.3 SET Pulse Width in Standard Delay Cells

Besides the most common logic gates analyzed in previous sections, complex gates composed of multiple primitive gates are also widely used in digital designs. One example of such a gate is the standard delay cell (SDC). **To our knowledge, our work introduces for the first time the analysis of SET effects in SDCs** [MA19]. The SDCs are used for timing synchronization in digital circuits. A typical example of a circuit which employs delay cells is the time-to-digital converter. In addition, the IC design tools insert the SDCs in logic paths to resolve the timing issues (hold time violations).

SDCs are designed as a serial connection of an even number of inverters based on skewed transistor sizing. In contrast to the sizing applied to other standard cells where the channel width of PMOS is larger than that of NMOS, in skewed gates the NMOS can be larger than the PMOS and also the channel length can be larger than the channel width. As a result, in skewed gates one logic transition (0-to-1 or 1-to-0) is

faster than the other. The use of SDC provides a cost-effective solution, as they are designed to generate the predefined delays (e.g. 500 ps, 1 ns, etc.) with the minimum number of cascaded inverters.

In this study, the SET pulse width at the output of two SDCs, denoted as SDC_x1 and SDC_x2, has been investigated using the same simulation setup as in previous analysis. The selected SDCs are designed as a serial connection of four inverters. The delays of SDC_x1 and SDC_x2 are 570 ps and 1.5 ns, respectively, and the cell areas are $15.9 \ \mu\text{m}^2$ and of $20.6 \ \mu\text{m}^2$, respectively. The transistor sizes for both SDCs are given in Table 4.9. In each cell the first and last inverters have standard size (PMOS transistor has twice larger channel width than NMOS transistor, and channel length is $0.13 \ \mu\text{m}$), while the second and third inverters are skew-sized (with the channel length greater than $0.13 \ \mu\text{m}$).

Inverter	SDC_x1 size (µm)	SDC_x2 size (µm)
Inverter 1	$W_P/L_P = 0.46/0.13, W_N/L_N = 0.3/0.13$	$W_{P}/L_{P} = 0.46/0.13, W_{N}/L_{N} = 0.3/0.13$
Inverter 2	$W_P/L_P = 1.27/0.7, W_N/L_N = 0.84/0.7$	$W_P/L_P = 1.29/1.25, W_N/L_N = 0.7/1.55$
Inverter 3	$W_P/L_P = 1.1/0.6, W_N/L_N = 0.84/0.5$	$W_P/L_P = 1.0/1.55, W_N/L_N = 0.84/1.2$
Inverter 4	$W_P/L_P = 1.29/0.13, W_N/L_N = 0.84/0.13$	$W_P/L_P = 1.29/0.13, W_N/L_N = 0.84/0.13$

Table 4.9: Channel width (W) and length (L) for NMOS (N) and PMOS (P) transistors in SDCs

In Figure 4.14, the SET pulse width at the output of SDC_x1 and SDC_x2 as a function of LET, for nominal supply voltage of 1.2 V and temperature of 27 °C, is presented. The bias-dependent current model was used to inject SETs successively in each inverter, for LET from 0.5 to 30 MeVcm²mg⁻¹. The results are for low level at the input of SDC. For high input level, the SET pulse widths are lower by around 200 ps. It can be seen that for both SDC designs, Inverter 2 and Inverter 3 are more sensitive than Inverter 1 and Inverter 4. The maximum SET pulse width is around 806 ps for SDC_x1 and around 1.46 ns for SDC_x2. Thus, upsizing the delay cell deteriorates its SET robustness. For both SDCs the SET pulses in Inverter 2 and Inverter 3 are already longer than 300 ps for LET = 1 MeVcm²mg⁻¹. Interestingly, Inverter 1 in SDC_x2 is immune to SETs in the investigated LET range, i.e., no SETs are observed at the output of the cell, and this can be attributed to the filtering effect of Inverter 2.

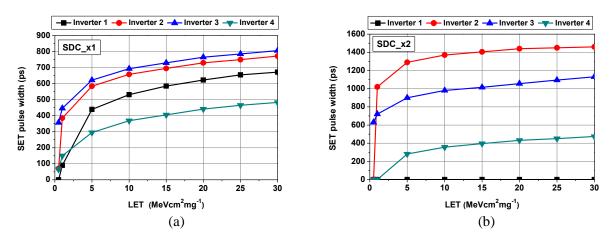


Figure 4.14: SET pulse width at the output of SDC_x1 and SDC_x2, when current pulse is injected successively in each inverter within the cells, for low input level

To evaluate the impact of supply voltage and temperature variations on the SET pulse width at the output of SDCs, the simulations have been done for three corner cases. The results for the most sensitive inverter in each SDC are shown in Figure 4.15. The SET pulse width increases for lowest supply voltage ($V_{DD} = 1.08 \text{ V}$) and highest temperature corner ($T_{EMP} = 125 \text{ °C}$), and this increase is more pronounced for SDC_x2 cell. Since SDC_x2 cell has larger skew sizing, these results confirm a strong correlation between the skew sizing and the SET sensitivity. It can be noticed that the supply voltage and temperature variations have stronger impact on SETs in skewed logic than in standard cells analyzed in previous sections.

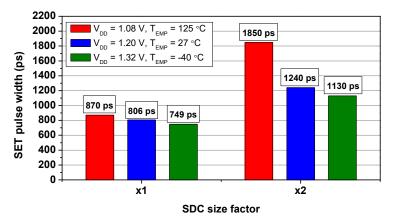


Figure 4.15: SET pulse width at the output of SDCs for supply voltage and temperature corners

4.3.3.4 Overall Comparison of SET Pulse Width

The SET pulse widths for all analyzed standard cells, for driving strength x1 and most sensitive input levels, when the current pulse with LET of 1, 10, 30 and 60 MeVcm²mg⁻¹ is injected successively in the output of each gate, are given in Table 4.10. These results have been obtained for nominal supply voltage (1.2 V), temperature of 27 °C and with INV_x1 as a load gate.

As can be seen, the most sensitive 2-input gates are NOR, XNOR and XOR, with the pulse widths greater than 600 ps for highest investigated LET. On the other hand, INV and BUF are the least sensitive. Note that the SET pulse in the case of NAND gate is longest for NAND4, while in the case of NOR gate it is shortest for NOR4. This difference is due to different gate structures. When the driving strength is increased from x1 to x2, the SET pulse width decreases by 50 - 100 ps for all gates over the investigated LET range. As in the case of critical charge, a strong impact of the number of inputs on the SET pulse width can be observed. For NAND and NOR gates, the output SET pulse width changes up to 50 % when the number of inputs increases. The obtained results can be utilized as a guideline for the rad-hard circuit designers in selecting the logic gates with highest robustness in terms of generated SET pulse width.

However, if the most sensitive node in each gate is considered, rather than the output node, than the SDC would be the most sensitive cell. The SET pulse widths for most sensitive nodes in standard cells with driving strength x1 are given in Figure 4.16. For SDC, the most sensitive nodes are the two internal skew-sized inverters. It can be observed that the SET pulses induced in SDC are almost 100 ps longer than those in other standard cells for LET = 30 MeVcm²mg⁻¹. It is interesting to note that by upsizing the SDC, the SET pulse width increases, as shown in Section 4.3.3.3. This effect is opposite to that for all other cells,

which become more robust when upsized. This indicates that the SDCs are potentially more sensitive to SETs than other standard cells in the investigated library. As the SET sensitivity due to skewed sizing is independent of technology, it can be expected that SDCs would be among the most vulnerable cells in any standard cell library. Thus, special SET mitigation measures are required for these cells.

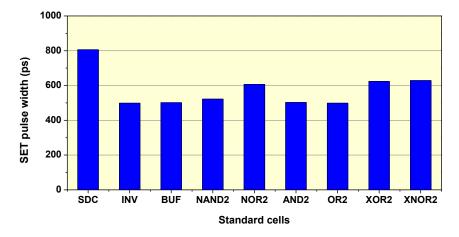


Figure 4.16: SET pulse width at the output of standard combinational cells with x1 driving strength, when the current pulse with LET = $30 \text{ MeV cm}^2\text{mg}^{-1}$ is injected in the most sensitive node

Gate type		SET pulse	width (ps)	
(most sensitive input level)	LET = 1 MeVcm ² mg ⁻¹	LET = 10 MeVcm ² mg ⁻¹	LET = 30 MeVcm ² mg ⁻¹	LET = 60 MeVcm ² mg ⁻¹
INV (0)	131	388	499	570
BUF (1)	131	390	502	572
AND2 (11)	132	392	503	573
AND3 (111)	130	293	504	575
AND4 (1111)	126	394	505	575
NAND2 (11)	143	403	522	593
NAND3 (111)	200	457	577	648
NAND4 (1111)	245	504	624	696
OR2 (11)	130	388	499	570
OR3 (111)	131	387	499	569
OR4 (1111)	0	305	415	486
NOR2 (00)	244	496	607	678
NOR3 (000)	323	575	686	756
NOR4 (0000)	131	390	501	572
XOR2 (10)	259	513	624	694
XOR3 (100)	263	514	626	696
XNOR2 (00)	265	519	629	700
XNOR3 (000)	329	578	691	761
SDC (0)	65	380	490	560

 Table 4.10: SET pulse widths at the outputs of standard cells with driving strength x1, when the current pulse is injected in the output node

4.4 SET Propagation Analysis

The SET pulse generated at the output of a logic gate will propagate through subsequent gates if there is an open (sensitized) logic path. As elaborated in Chapter 2, the SET propagation scenarios include complete filtering (electrical masking), broadening and shrinking (attenuation) of SET pulse. In this section, the SET propagation in terms of design and operating parameters is analyzed, while the corresponding SET propagation model derived from the simulation results is presented in Section 4.6.3.

In order to ease the analysis, certain simplifications have been applied. Namely, we have analyzed only the SET pulse width for the maximum SET amplitude. Although the initial SET pulse may have any amplitude within the power supply rails, after propagation through a single logic stage it will attain the maximum value (equal to supply voltage). Moreover, with technology scaling, the full-swing SET pulses can be generated by the low-LET particles, and this was also confirmed for the investigated 130 nm technology, as shown in Figure 4.9. For this reason, we consider that the propagation of SET pulses with the maximum amplitude as the most critical case for SET analysis. Nevertheless, the presented analysis can be extended to include the SET amplitude. The effects of SET propagation are analogous to the propagation of any digital pulse, and the main difference is in the pulse width. Normal signals propagating through digital logic are usually at least several ns wide, whereas the SET pulse width is in the range of hundreds of ps. The SET broadening/narrowing is also affected by the reconvergent paths, i.e., the circuit topology, but that scenario is not considered in this work.

For this analysis the symmetric SET voltage pulse, with 10 ps rise and fall time constants, was fed to the input(s) of each investigated gate. It is important to note that real SET pulses are usually asymmetric, where the fall time is longer than the rise time. As a result of asymmetry in the rise and fall time constants, the SET pulse can be wider than in the case with equal rise and fall time constants, but this does not diminish the generality of the adopted approach. The performed characterization can be easily extended with more parameters to obtain more detailed information. In this case the input pulse widths up to 600 ps have been used, as this is the typical SET pulse width range for the investigated technology.

As the propagation delay is the primary measure of the gate's electrical masking capacity, initially all standard cells have been characterized to obtain their propagation delay for different operating settings. This was done by traversing a fixed pulse of 1 ns through the gates. All studied gates have the propagation delay lower than 115 ps, for nominal supply voltage and temperature, and minimum-sized load inverter. The basic gates (INV, NAND2 and NOR2) have the propagation delay below 30 ps. The 2-input gates AND2, OR2, XOR2 and XNOR2 have the propagation delay from 30 to 90 ps, while the 3- and 4-input gates have the propagation delay up to 115 ps. By doubling the driving strength of any gate, the propagation delay decreases by a maximum of 10 ps. The standard delay cells have the largest propagation delay, from 500 ps to 2 ns depending on the cell configuration.

4.4.1 SET Propagation through Single-Input Gates

The single-input gates INV and BUF are particularly critical from the perspective of SET propagation, because they have no logical masking capability. Both gates cause minor broadening of positive input pulses and shrinking of negative input pulses, for the input pulse widths greater than 50 ps. The magnitude

of broadening and shrinking caused by INV_x1 is approximately 5 ps for the entire input pulse width range, while BUF_x1 causes the broadening or shrinking of 8 ps for the same input pulse widths. The tendency of logic gates to broaden the pulses with one polarity, and shrink the pulses with opposite polarity, has been confirmed in previous studies [133, 154]. It has been shown that a given logic gate causes almost the same magnitudes of pulse broadening and shrinking, and these effects are related to the imbalance between high-to-low and low-to-high transition times.

As the gate's driving strength increases, the propagation delay is reduced, resulting in further broadening or shrinking of the propagating SET pulse, depending on the input pulse polarity. The dependence of the output pulse width on the driving strength of INV and BUF gates, for the input pulse of 200 ps, is shown in Figure 4.17. In both cases, the load is a single INV_x1 gate and the supply voltage and temperature are 1.2 V and 27 °C, respectively. The output SET pulse width changes from 4 to 15 ps with the driving strength, and the relation between the output SET pulse width and the driving strength can be well fitted to a power law, with the correlation coefficient $R^2 > 0.9$. Similar behavior was observed for all input pulse widths. Note that this dependence would not be valid for input pulses shorter than 50 ps, as in that case the electrical masking of (attenuation of SET pulse amplitude) would be more pronounced, whereby the BUF gate has better masking property due to larger delay.

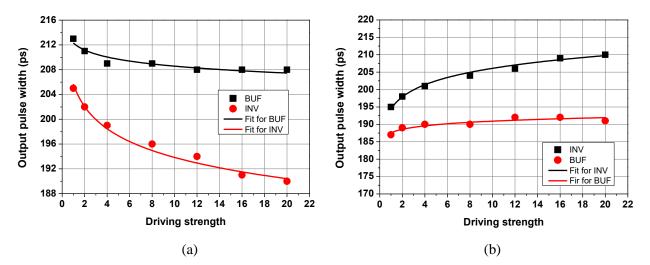


Figure 4.17: SET pulse width at the output of INV and BUF gates, as a function of their driving strength, for: (a) positive input pulse of 200 ps, (b) negative input pulse of 200 ps

Similarly, the variation of load size affects the propagation delay, and thus the SET pulse width. Since the output pulse width is observed at the output pin of target gate, the impact of load size can be regarded in terms of the total load capacitance. By changing the number or type of load gates, the load capacitance is also changed. Thus, we express the output SET pulse width in terms of the capacitance of load gates. This allows to identify the impact of different load gates in terms of their input capacitance. For example, NAND2_x1 has the same input capacitance as INV_x1. The input capacitance for standard logic gates is available in the library characterization file .LIB.

The impact of load capacitance on the propagated SET pulse width, for INV_x1, INV_x2 and INV_x4 gates, and input pulse width of 200 ps, is illustrated in Figure 4.18. The load capacitance was varied by

increasing the driving strength of a single INV load gate from x1 to x12, which results in the change of load capacitance from 4 to 55 fF. This range of load capacitance is typical for most modern designs. The output pulse width increases for positive input pulses, and decreases for negative input pulses. In the case of BUF gates the reverse behavior was observed, and hence this is not shown here for brevity. The dependence of output SET pulse width on load capacitance can be fitted to a linear relation. However, as can be seen, for negative input pulse the dependence deviates from linear as the load capacitance is increased, and can be better fitted to a power law. Note that the impact of load capacitance on the SET propagation is stronger than that of the driving strength of target gate. This deviation is attributed to the filtering effects of larger load capacitance. It is particularly important to emphasize that while the change of driving strength of a particular gate can change the propagated SET pulse width by less than 10 %, the change of load capacitance can cause the variation of SET pulse width by more than 10 %.

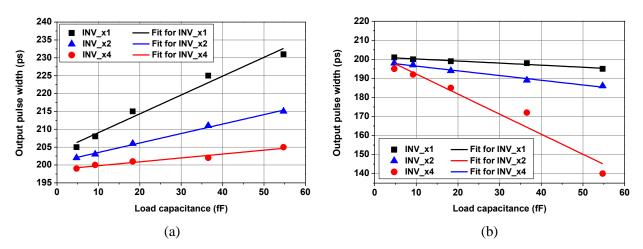


Figure 4.18: SET pulse width at the output of INV gate, as a function of its driving strength and load capacitance, for: (a) positive input pulse of 200 ps, (b) negative input pulse of 200 ps

In Table 4.11 and Table 4.12, the SET pulse width at the output of INV_x1 and BUF_x1 gates, for different supply voltages and positive input pulse widths, is given. The output pulse width changes by approximately equal value for positive and negative input pulses. For positive input SET pulses wider than 200 ps, the output SET pulse width increases by 1 - 4 ps for INV_x1, and 3 - 8 ps for BUF_x1, for each decrease in supply voltage by 0.1 V. Conversely, for negative input pulse, the SET width decreases by the same magnitude. It is important to note that the change of SET pulse width is more pronounced at lower supply voltage. For input pulse width above 100 ps, the SET pulse width changes are independent of the input pulse width. However, it should also be noted that reducing the supply voltage reduces the propagation delay, and thus the minimum input pulse width that can propagate decreases.

The impact of temperature on the SET propagation through INV and BUF gates with driving strengths x1 and x2 is shown in Table 4.13. The change of SET pulse width is 2 - 6 ps over the temperature range from -40 to 125 °C. However, as this is the change of SET pulse width only for a single gate, the overall SET pulse width variation may be larger in a long chain composed of these gates, particularly in chains with high affinity for the propagation-induced pulse broadening. As will be demonstrated in Section 4.4.2, the impact of temperature may be more significant for multi-input logic gates.

Pulse width for positive	Output pulse width (ps)						
input pulse (ps)	$V_{DD} = 0.8 V$	V _{DD} = 0.9 V	$V_{DD} = 1 V$	V _{DD} = 1.1 V	V _{DD} = 1.2 V		
100	115	111	108	106	105		
200	215	211	208	206	205		
300	315	311	308	306	304		

Table 4.11: SET pulse width at the output of INV_x1 in terms of supply voltage, for positive input pulses

Table 4.12: SET pulse width at the output of BUF_x1 in terms of supply voltage, for positive input pulses

Pulse width for positive	Output pulse width (ps)						
input pulse (ps)	V _{DD} = 0.8 V	$\mathbf{V}_{\mathrm{DD}} = 0.9 \ \mathbf{V}$	$V_{DD} = 1 V$	V _{DD} = 1.1 V	V _{DD} = 1.2 V		
100	95	114	115	115	113		
200	235	227	220	216	213		
300	335	327	320	316	313		

Table 4.13: SET pulse width at the outputs of INV and BUF gates, in terms of temperature, for $V_{DD} = 1.2$ V and positive input pulse of 200 ps

Cata trima	Output SET pulse width (ps)					
Gate type	T_{EMP} = - 40 °C	$T_{EMP} = 27^{\circ}C$	$T_{EMP} = 125 \ ^{\circ}C$			
INV_x1	206	205	204			
INV_x2	208	210	214			
BUF_x1	213	213	212			
BUX_x2	215	217	219			

4.4.2 SET Propagation through Multiple-Input Gates

For multiple-input logic gates, the width of propagated SET pulse strongly depends on the input pattern, i.e., the input pin at which the SET pulse arrives [90]. That is because different input patterns activate different transistors within the gate, and thus lead to different equivalent resistance. In the case of multi-input cells with logical masking capability (all cells except XOR and XNOR), only the input patterns which do not cause logical masking are considered. For multi-input cells investigated in this work, the simulations have shown that the output SET pulse width varies by a maximum of \pm 10 ps depending on the input pin at which the SET arrives. Without loss of generality, the results presented in this section are for the SET pulse propagating through one input of a logic gate.

The effect of SET propagation through multiple-input gates is qualitatively similar as in the case of single-input gates, i.e., equal magnitude of broadening or shrinking occurs for opposite polarities of input pulse with sufficient width. However, the gate complexity has dominant influence on the SET propagation through multiple-input gates. The complex gates such as AND and OR have larger propagation delay than the basic gates NAND and NOR, and thus are more effective in SET suppression. This is illustrated in

Figure 4.19 for NAND and AND gates with 2, 3 and 4 inputs. For example, the SET pulses shorter than 100 ps are only partly attenuated by AND3 gate, but completely filtered by AND4 gate. It can be noticed that AND gate has better filtering capability. For both NAND and AND gates, the variants with larger number of input pins have better filter capability. The dependence of SET pulse width on driving strength of target gate and load capacitance follows similar relations as for the single-input gates. By increasing the driving strength to x4, the pulse width increases or decreases by 5 - 10 ps, depending on the type of gate. However, with a load inverter x12, the pulses shorter than 200 ps can be significantly suppressed or completely filtered for one input polarity.

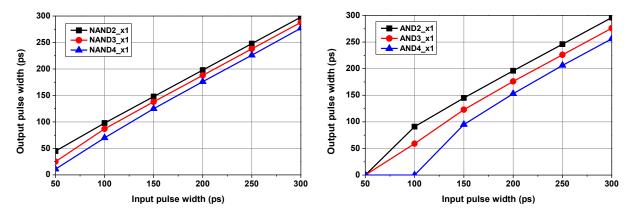


Figure 4.19: SET pulse width at the output of 2-, 3- and 4-input NAND and AND gates, as a function of input SET pulse width

The dependence of SET pulse width at the output of NAND and AND logic gates on supply voltage is given in Table 4.14. With the increasing number of inputs, i.e. increasing gate complexity, the magnitude of SET pulse broadening/shrinking increases. Similar trend was observed for other gates with multiple inputs. The increase or decrease of output SET pulse width in terms of supply voltage, for a particular gate, can be fitted to a power law, as in the case of single-input gates. It is important to note that SET propagation through a multi-input gate is more sensitive to supply voltage than the single-input gates. As can be seen in Table 4.14, at supply voltage lower than 0.9 V, the SET pulse width decreases significantly or is completely filtered. The effect is opposite for negative input pulse polarity.

		Overall change				
Gate type	$V_{DD} = 0.8 V$	V _{DD} = 0.9 V	$V_{DD} = 1 V$	V _{DD} = 1.1 V	V _{DD} = 1.2 V	of SET pulse width (ps)
NAND2_x1	191	196	198	199	198	7
NAND3_x1	140	170	180	185	188	48
NAND4_x1	84	137	160	171	176	92
AND2_x1	136	181	191	194	196	60
AND3_x1	0	111	153	169	176	176
AND4_x1	0	0	101	136	153	153

Table 4.14: SET pulse width at the output of NAND and AND gates, in terms of supply voltage,
for positive input pulse of 200 ps

Similarly, the temperature variations exhibit stronger impact on gates with larger number of inputs, as shown in Table 4.15. However, the impact of temperature is weaker than that of supply voltage. As temperature changes from -40 to 125 °C, the SET pulse width changes by 3 to 21 ps during propagation through NAND and AND gates. Note that the temperature variation has stronger impact on multiple-input gates than on single-input gates. Even though the change of SET pulse width for 2-input gates is relatively small for both supply voltage and temperature variations, the accumulation of pulse broadening or shrinking through a particular logic path can cause significant change of the output SET pulse width. This is demonstrated in Section 4.4.4.

for positive input pulse of 200 ps							
Gate type	Outp	Output SET pulse width (ps)					
	T _{EMP} = - 40 °C	$T_{EMP} = 27 \ ^{\circ}C$	$T_{EMP} = 125 ^{\circ}C$	of SET pulse width (ps)			
NAND2_x1	198	197	195	3			
NAND3_x1	191	199	184	7			
NAND4_x1	181	176	170	11			
AND2_x1	199	197	193	6			
AND3_x1	186	182	175	11			
AND4_x1	162	153	141	21			

Table 4.15: SET pulse width at the outputs of NAND and AND gates, in terms of temperature, for positive input pulse of 200 ps

4.4.3 Overall Comparison of SET Propagation Effects

The presented results have shown that the SET propagation through a single logic gate is predominantly influenced by the SET pulse polarity and supply voltage. Although the impact of gate size and temperature is weaker, the contribution of all parameters must be considered for accurate evaluation of SET propagation. It has been demonstrated that the SET pulse width changes by almost equal magnitude for both polarities of input pulse. These observations are the key for establishing an analytical model for the propagation-induced SET pulse broadening/shrinking, as will be detailed in Section 4.6.

In the rad-hard design process it is important to quantify the electrical masking and the PIPB effect for each gate in order to select the most appropriate design configuration. The SET propagation capacity of the analyzed gates with driving strength x1 is shown in Table 4.16. The values shown in red denote the cases when the SET pulse is either completely filtered or significantly attenuated (pulse width is decreased by at least two times). As can be observed, the SET pulses of 50 ps are attenuated or filtered in most cases, particularly the negative pulses. The input pulses longer than 100 ps can propagate through most logic gates, with certain shrinking or broadening. As the input pulse width increases, the shrinking/broadening induced by individual gates is uniform across the investigated pulse width range. The best electrical masking (significant attenuation or complete filtering) is exhibited by complex gates. However, the gates with the best electrical masking have the strongest pulse broadening affinity for opposite pulse polarity. This is directly related to the propagation delay of the respective gates, as larger propagation delay implies larger degradation of short pulses. These results are essential for estimating the propagation effects through the combinational paths composed of analyzed logic gates.

Gate		ulse width for put pulse (ps	-	Output pul inp	se width fo out pulse (p	
type	Input = 50 ps	Input = 100 ps	Input = 200 ps	Input = 50 ps	Input = 100 ps	Input = 200 ps
INV	55	105	205	45	95	195
BUF	51	113	213	0	86	187
SDC	0	0	0	0	0	0
NAND2	43	98	198	49	102	202
NAND3	25	87	188	52	112	212
NAND4	11	70	176	53	122	223
NOR2	77	128	228	14	70	172
NOR3	101	154	254	0	39	146
NOR4	95	161	265	0	0	134
AND2	0	91	196	0	101	204
AND3	0	59	176	0	117	224
AND4	0	0	153	0	132	244
OR2	85	156	257	0	18	142
OR3	0	200	303	0	0	88
OR4	89	163	265	0	0	133
XOR2	43	109	218	0	52	179
XOR3	0	102	212	0	68	186
XNOR2	27	97	198	33	101	202
XNOR3	54	144	247	0	30	148

Table 4.16: SET pulse widths at the outputs of logic gates, for positive and negative input pulses of 50, 100 and 200 ps (for driving strength x1, INV_x1 as a load gate, $V_{DD} = 1.2$ V and $T_{EMP} = 27$ °C)

4.4.4 SET Propagation in Combinational Paths

Although the variation of SET pulse width after propagation through a single gate is in most cases less than 40 ps, the SET pulse width at the output of a logic path may be significantly longer than the input pulse width as a result of accumulated SET pulse broadening. Alternatively, the accumulation of SET shrinking can result in significant suppression or complete filtering of SET pulse. In order to investigate the SET propagation effects in terms of logic path structure and supply voltage and temperature corners, we have performed the simulations for ten characteristic logic paths, as shown in Table 4.17. In contrast to previous reports which have analyzed the paths composed of tens or hundreds of gates [87 - 90], we have studied the paths with only 10 gates because such short paths are most common in modern digital designs.

Two types of logic paths have been investigated: (i) paths composed of the same type of gates, and (ii) paths composed of different types of gates. As previous works [87, 88] have confirmed that the logic paths composed of gates with different driving strength may cause significant SET broadening or shrinking, in this case we have analyzed only the paths made of gates with the same driving strength (x1). The analysis was done for three corner cases for supply voltage and temperature: (i) low-VT corner (LVT), i.e., $V_{DD} = 1.08$ V and $T_{EMP} = -40$ °C, (ii) typical-VT corner (TVT), i.e., $V_{DD} = 1.2$ V and $T_{EMP} = 27$ °C, and (iii) high-

VT corner (HVT), i.e., $V_{DD} = 1.32$ V and $T_{EMP} = 125$ °C. The SET propagation was analyzed with positive and negative input pulses of 200 ps.

Table 4.17: SET pulse width at the outputs of combinational paths, for positive and negative input pulses
of 200 ps, for LVT ($V_{DD} = 1.08 \text{ V}$, $T_{EMP} = -40 \text{ °C}$), TVT ($V_{DD} = 1.2 \text{ V}$, $T_{EMP} = 25 \text{ °C}$), and
HVT ($V_{DD} = 1.32 \text{ V}, T_{EMP} = 125 ^{\circ}\text{C}$)

10-gate combinational paths	Output pulse width (ps)							
(all gates are with driving	Positive i	nput pulse	= 200 ps	Negative input pulse = 200 ps				
strength x1)	LVT	TVT	HVT	LVT	TVT	HVT		
INV	208	206	204	195	196	197		
BUF	367	322	293	0	68	108		
NAND2	201	201	201	203	204	204		
AND2	166	152	134	237	250	268		
NOR2	223	216	214	151	176	185		
OR2	925	748	645	0	0	0		
Alternating OR2 and AND2	542	447	387	0	0	0		
Alternating AND3 and OR4	499	416	359	0	0	0		
Alternating NAND2 and NOR3	667	563	506	0	0	0		
Alternating XNOR3 and NOR2	0	0	0	173	243	252		

The results in Table 4.17 indicate two major trends for the dependence of SET propagation on the path structure, for the typical supply voltage and temperature case (TVT). First, in a path composed of the same type and driving strength of inverting gates (INV, NAND, NOR), negligible broadening or shrinking of SET pulse occurs. That is because the SET pulse polarity changes though each inverting gate, resulting in alternating pulse broadening and shrinking. Second, in a path composed of non-inverting gates of the same type and driving strength (BUF, AND, OR) or different types of gates, significant broadening or shrinking, or even filtering, of the SET pulse may occur. This is a valuable reference for the rad-hard design process, indicating the need to particularly address the non-inverting combinational paths.

For LVT and HVT corners, the variation of propagated SET pulse width due to supply voltage and temperature variations is also most pronounced for paths composed of the same type of non-inverting gates or different types of gates. As can be seen in Table 4.17, between the low-VT and high-VT corners, the SET pulse width changes for more than 60 ps at the output of BUF path, for approximately 30 ps at the output of AND2 path, and for almost 300 ps at the output of OR2 path. In the case of paths composed of different gate types, the SET pulse width changes for more than 100 ps between the two extreme corners. This shows that it is especially important to take into account the combined impact of supply voltage and temperature variations on the SET propagation.

It is important to note that the overall SET broadening or shrinking across a logic path can be estimated by algebraic summation of the broadening or shrinking induced by individual gates in the path. For example, according to the results given in Table 4.16 and Table 4.17, in the case of logic paths composed of the same type and size of non-inverting gates, the overall SET pulse broadening or shrinking for 10-gate paths is roughly equal to the product of the pulse broadening/shrinking of individual gates and the number of gates in the path. Therefore, provided an appropriate model for estimating the SET broadening and shrinking for individual gates is available, the SET propagation effects in a given combinational path can be assessed analytically (without additional simulations).

4.5 SET-Aware Design Considerations

The results presented in previous sections have shown that the investigated standard cells exhibit differing sensitivity in terms of SET generation and propagation. Moreover, the change of design, operating and irradiation parameters may cause the variation of SET sensitivity over a wide range. This fact can be exploited to guide the synthesis tools to reduce the usage of highly sensitive cells or replace them with the less sensitive cells or alternative logic implementations. In addition, the characterization results can be used as a guideline in selecting the most appropriate gate-level SET mitigation strategy. Based on the acquired results, the following general guidelines for the SET-aware design can be defined:

- The standard delay cells based on skewed inverters are the most vulnerable standard cells. Due to skew sizing of two internal inverters, the SETs longer than 1 ns can be generated when a particle strikes these inverters. Two options can be considered to mitigate such long SETs. First solution is to replace the SDC with delay lines realized with standard inverters, provided the introduced area overhead does not violate the area constraints. The second option is to apply appropriate gate-level SET mitigation technique, as will be discussed in Section 5.6.
- Concerning the SET generation in 2-input gates, the most sensitive are NOR2, XNOR2 and XOR2 gates. These gates have the highest nominal SER, and can potentially generate longest SETs. Therefore, the use of these gates in the design should be minimized whenever possible. If these gates are used in combinational paths with low logical masking probability, special gate-level hardening measures have to be applied to these gates in order to suppress the SET pulses.
- There is no a clear correlation between the SET generation sensitivity and the number of inputs. For example, NAND4 is more sensitive than NAND3 for all low input levels, but the response is opposite for all high input levels. This difference comes from the fact that the designs for 3- and 4- input gates differ depending on the type of gate.
- From the aspect of SET propagation, the SETs longer than 200 ps can propagate through almost all logic gates. Though, it is not possible to identify the most sensitive gates because the same gate can broaden or shrink the propagating SET pulse, depending on the polarity of the pulse. The NOR2, OR2 and XOR2 gate are the most sensitive gates in terms of SET pulse broadening, while gates with more inputs have better SET filtering capability. The paths composed of non-inverting gates are especially prone to SET pulse broadening.
- The combined impact of gate size, input logic levels, supply voltage and temperature may cause the variation of nominal SER per gate of at least one order of magnitude. Furthermore, the variation of these parameters may cause the change of generated or propagated SET pulse width by more than 40 %. Therefore, considering the combined impact of the aforementioned parameters in the early design phase is imperative.

4.6 SET Sensitivity Models

The characterization results for each gate are organized in the form of 2-dimensional LUTs, such that each LUT represents the variation of one SET sensitivity metric (critical charge, generated SET pulse width) or propagated SET pulse width) in terms of two parameters. For example, one LUT stores the critical charge values for INV gate in terms of its driving strength and driving strength of one type of load gate, for nominal values of all other parameters. Similarly, the LUTs for generated and propagated SET pulse widths are constructed for each logic gate type. The total number of LUTs per gate type depends on the number of parameters that are analyzed during the characterization. More details on the total number of required LUTs for storing all characterization data are given in Section 4.8.

In order to reduce the complexity of subsequent evaluation of SET generation and propagation in a given circuit, appropriate analytical models are derived from the characterization LUTs. The analytical models offer two main benefits: (i) reduction of the characterization data, and thus the required memory for storage of characterization database, (ii) reduction of time for reading the database, and thus faster subsequent SET analysis. To this end, we have adopted the modeling approach based on analytical fitting of simulation results. In contrast to the physics-based models, the fitting models capture the most important parameters affecting the SET sensitivity, while the technological parameters are transparent to the designer. Thus, the models can be adopted to different technologies by performing the necessary characterization, without the need to have access to technological parameters, which are often proprietary. As shown in previous discussion, the value of any SET metric increases or decreases proportionally to the increase or decrease of the values of contributing parameters. Therefore, the proposed models have been constructed employing the principle of superposition. Such modeling approach provides essential benefits over existing models presented in Section 3.3. By employing the principle of superposition, it is possible to assess both individual and combined impacts of contributing parameters, which can help the designers to identify the optimal design and operating conditions. In contrast to SET existing models that employ the transistor size (channel width and length) as a model parameter, we express the SET metrics as a function of the driving strength (size factor) of logic gates. As a result, the gate structure is transparent to the designer, thus simplifying the analysis as the transistor sizes are not explicitly considered in the design phase.

4.6.1 Critical Charge Model

This section introduces a critical charge model derived by fitting the characterization results presented in Section 4.3.1. According to the performed characterization, the general form of the critical charge model as a function of five analyzed parameters can be expressed as,

$$Q_{CRIT} = f(S_T, S_L, C_L, V_{DD}, T_{EMP})$$
(4.1)

where the model parameters S_T , S_L , C_L , V_{DD} and T_{EMP} denote the size factor of target gate, size factor of load gate, additional load capacitance, supply voltage and temperature, respectively. According to the general setup depicted in Figure 4.2, a load gate with size factor S_L is a gate at whose output the critical charge is determined. The additional load capacitance is the sum of the capacitance of interconnection wires and additional load gates (if fanout > 1). For fanout > 1, different values of critical charge can be obtained at the outputs of different load gates. Recall that the size factors S_T and S_L are numerical representations of driving strength, adopted in order to ease the mathematical modeling and eliminate the need for considering the transistors sizes in the model. It is important to note that the critical charge model defined by the general relation (4.1) is derived for fixed values of timing parameters of the injected current pulse, fixed input levels and a single sensitive node in the target gate. The same modeling concept can be applied to different current pulse parameters, input levels and sensitive nodes.

The obtained simulation results in Section 4.3.1 have shown that the dependence of critical charge on each parameter is almost linear (with some deviations for supply voltage and temperature). Moreover, the slope of the relation between critical charge and any parameter is determined by other contributing parameters. In that regard, using the principle of superposition, the critical charge can be defined as the sum of multiple contributing factors. The general relation (4.1) can therefore be rewritten to express the Q_{CRIT} dependence on N analyzed parameters ($K_1, ..., K_N$) as follows [MA15],

$$Q_{CRIT} = Q_{NOM} + \sum_{i=1}^{N} f_i \cdot (K_i - K_{iNOM}) + f_{ERROR}$$
(4.2)

In relation (4.2), Q_{NOM} denotes the value of critical charge when all parameters K_i are at nominal values K_{iNOM} . The notation K_i represents the parameters S_T , S_L , C_L , V_{DD} and T_{EMP} . Q_{NOM} is obtained directly from simulations and has a unique value for each gate type, sensitive node within the gate, input logic levels and timing parameters of the current pulse. f_i are the linear fitting functions representing the contribution of parameters K_i on the value of Q_{CRIT} . As any parameter K_i increases or decreases with respect to its nominal value K_{iNOM} , the value of Q_{CRIT} will increase or decrease accordingly, as has been demonstrated in previous discussion. To compensate for the non-linearity between Q_{CRIT} and size factor S_T , an additional fitting function f_{ERROR} is introduced. For the gates investigated in this case, the nonlinearity occurs only for INV and BUF, and the function f_{ERROR} is a linear fitting function.

Considering that the proposed model defines the critical charge in terms of five contributing parameters, the relation (4.2) can be formulated as,

$$Q_{CRIT} = Q_{NOM} + f(S_T) + f(S_L) + f(C_L) + f(V_{DD}) + f(T_{EMP}) + f_{ERROR}$$
(4.3)

 $f(S_T)$ represents the increase of critical charge due to the increase of S_T (i.e. for $S_T > 1$), for $S_L = 1$, $C_L = 0$, $V_{DD} = V_{DD_NOMINAL} = 1.2$ V and $T_{EMP} = T_{EMP_NOMINAL} = 27$ °C. Thus, this relation can be expressed as,

$$f(S_T) = a_0 \cdot (S_T - 1) \tag{4.4}$$

where the coefficient a_0 is determined by linear fitting of dependence between critical charge and S_T , as follows,

$$a_0 = \frac{Q_{CRIT}(S_T = n) - Q_{CRIT}(S_T = 1)}{n - 1}$$
(4.5)

In relation (4.5), *n* denotes the maximum size factor for each gate. For the investigated library, n = 40 (for inverter), n = 20 (for buffer) and n = 8 (for all other gates).

 $f(S_L)$ represents the increase of critical charge when S_L is increased (i.e. for $S_L > 1$), for $C_L = 0$, $V_{DD} = V_{DD_NOMINAL} = 1.2$ V and $T_{EMP} = T_{EMP_NOMINAL} = 27$ °C. Analogously to relation (4.4), the impact of S_L on critical charge can be expressed as,

$$f(S_L) = a_1 \cdot (S_L - 1) \tag{4.6}$$

where the coefficient a_1 can be determined from the fitting relation (4.5), by replacing S_T with S_L . Note that the value of a_1 varies with the type of load gate.

 $f(C_L)$ represents the increase of critical charge due to additional load gates (if any) and interconnection wires, for $V_{DD} = V_{DD_NOMINAL} = 1.2$ V and $T_{EMP} = T_{EMP_NOMINAL} = 27$ °C. Thus, it is defined as a linear sum of load and wire capacitances,

$$f(C_L) = a_2 \cdot \sum_{i=1}^{N+1} C_L(i) = a_2 \cdot \left(C_W + \sum_{i=1}^N C_{IN}(i) \right)$$
(4.7)

where the coefficient a_2 can be determined by linear fitting of dependence between critical charge and total capacitance of additional load gates and interconnection wires.

 $f(V_{DD})$ denotes the change of critical charge when supply voltage increases or decreases with respect to $V_{DD_-NOMINAL}$. This term introduces a charge component which is subtracted from Q_{CRIT} when the supply voltage is lower than $V_{DD_-NOMINAL}$, and added to Q_{CRIT} when the supply voltage is higher than $V_{DD_-NOMINAL}$, and added to Q_{CRIT} when the supply voltage is higher than $V_{DD_-NOMINAL}$. It also takes into account the impact of size factors S_T and S_L on the dependence between critical charge and supply voltage, for $T_{EMP} = T_{EMP_-NOMINAL} = 27$ °C. Thus, $f(V_{DD})$ can be expressed as,

$$f(V_{DD}) = f(S_T, S_L) \cdot \left[V_{DD} - V_{DD_NOMINAL} \right]$$
(4.8)

$$f(S_T, S_L) = a_3 \cdot S_T + a_4 \cdot (S_L - 1)$$
(4.9)

where the coefficient a_3 represents the impact of S_T on the slope of relation (4.8), while the coefficient a_4 represents the impact of S_L on the slope of relation (4.8).

 $f(T_{EMP})$ accounts for the change of critical charge when temperature increases or decreases with respect to $T_{EMP_NOMINAL}$. Because Q_{CRIT} is inversely related to temperature, the term $f(T_{EMP})$ has a positive sign (+) for temperatures lower than $T_{EMP_NOMINAL}$ and a negative sign (-) for temperatures higher than $T_{EMP_NOMINAL}$. This term also takes into account the impact of size factor of target gate S_T and supply voltage V_{DD} on the relation between Q_{CRIT} and T_{EMP} . Since S_L has minor impact in this case, it could be neglected. Thus, $f(T_{EMP})$ can be expressed as,

$$f(T_{EMP}) = f(S_T, V_{DD}) \cdot \left[T_{EMP} - T_{EMP_NOMINAL}\right]$$
(4.10)

$$f(S_T, V_{DD}) = a_5 \cdot S_T + a_6 \cdot (V_{DD} - V_{DD_NOMINAL})$$
(4.11)

where the coefficient a_5 represents the impact of S_T on the slope of relation (4.10), while the coefficient a_6 accounts for the impact of V_{DD} on the slope of relation (4.10).

Based on relations (4.1) – (4.11), 8 model coefficients (Q_{NOM} and $a_0 - a_6$) are obtained for each type of logic gate. A single LUT can store the model coefficients for one gate type, all input levels, one sensitive node in the gate, one load gate type and predefined values of current pulse timing constants. Additional LUTs are required to store the coefficients for each combination of sensitive nodes, load gates and timing constants of current pulse.

The proposed modeling approach based on superposition principle is similar to the one reported by Rossi *et al.* [219], defined by the relation (3.8) in Section 3.3.2. However, in contrast to the model in [219], which considers only the transistor sizes of target and load gates, our model takes into account five contributing parameters. In comparison to previous models [217 - 219], our model expresses the critical charge in terms of design parameters, without involving explicitly any technological parameters. Furthermore, the main benefit of modeling based on superposition principle is the possibility to analyze the individual impact of each parameters, which may be related to the target technology. For example, it was shown in previous discussion that the dependence between critical charge and size factor of target gate is non-linear for certain gates and input levels.

In order to assess the accuracy of the proposed model with respect to the results from SPICE simulations, the comparison for each gate type was done for a number of settings. Table 4.18 shows the results for INV, NAND2 and NOR2 gates. It can be seen that the relative error of the proposed model with respect to the results from SPICE simulations is in most cases below 10 %, which is a very good accuracy. For minimum values of supply voltage and temperature, the error was up to 20 % for some gates. That is due to the non-linearity between critical charge and supply voltage (temperature), as discussed in Section 4.3.1. The model is compared to simulations only, and not to previous models [217 - 219], because the existing models are based on different modeling approaches, do not consider all parameters as in this case, and some of them require the technological parameters.

	Sim	ulation cond	litions		SPICE	Proposed	Relative
Target gate	Input level(s)	Load	Supply voltage (V)	Temp. (°C)	simulations (fC)	model (fC)	error (%)
INV_x2	0	INV_x2	1	80	46.9	51.7	10.2
INV_x8	1	INV_x4	1.1	20	198.6	202.2	1.8
INV_x4	0	INV_x1	1.2	50	128.3	133.4	4.0
NAND2_x1	01	INV_x1	0.9	-20	22.1	25.1	13.6
NAND2_x2	11	INV_x2	1.32	80	66.9	70.2	4.9
NAND2_x1	00	INV_x4	1.2	30	75.5	79.3	5.0
NOR2_x1	00	INV_x2	1.2	-10	25.5	27.9	9.4
NOR2_x2	10	INV_x1	1	100	63.4	66.7	5.2
NOR2_x2	01	INV_x1	1.1	0	81.4	85.1	4.5

Table 4.18: Comparison of critical charge obtained with proposed model and SPICE simulations, for different settings for INV, NAND2 and NOR2 gates

4.6.2 Generated SET Pulse Width Model

The purpose of an SET pulse width model is to predict the variation of SET pulse width generated in a logic gate in terms of various contributing parameters, and for $LET > LET_{TH}$. The value of LET_{TH} can be estimated from the critical charge, since the ratio between these two values is constant according to relation (2.2) (see Section 2.1). Thus, it is sufficient to obtain the ratio between Q_{CRIT} (determined with double-exponential current model) and LET_{TH} (determined with bias-dependent current model) for one gate, and then the value of LET_{TH} can be calculated from Q_{CRIT} values for different settings.

Based on the results in Section 4.3.2, we have defined analytical model for predicting the generated SET pulse width T_{SET} in terms of six contributing parameters. Analogously to the critical charge model, the SET pulse width model defines the width of the SET pulse generated in a target gate and propagated through the respective load gate. A generalized form of the model can be expressed as,

$$T_{SET} = f(LET, S_T, S_L, C_L, V_{DD}, T_{EMP})$$

$$(4.12)$$

where *LET*, S_T , S_L , C_L , V_{DD} and T_{EMP} denote the incident particle *LET*, size factor of target gate, size factor of load gate, total capacitance of interconnections and inputs of additional load gates (if fanout > 1), supply voltage and temperature, respectively. Similarly to the critical charge model, the SET pulse width model is derived for current injection in a single node in the target gate, one input vector and predefined timing parameters of the SET current pulse. The fitting procedure described in the following discussion has to be repeated for all combinations of target nodes, input vectors and current pulse timing parameters.

From the observations in Section 4.3.2, the width of the generated SET pulse can be modeled employing a similar superposition approach as for the critical charge. Therefore, the model defined by relation (4.12) can be expressed as a sum of four components,

$$T_{SET} = f(LET, S_T) + f(S_L, C_L) + f(V_{DD}) + f(T_{EMP})$$
(4.13)

The first component of expression (4.13) defines the SET pulse width in terms of two parameters, *LET* and S_T , for nominal values of all other parameters ($C_L = 0$, $V_{DD} = 1.2$ V and $T_{EMP} = 27$ °C). This form has been chosen because, according to our characterization results, the dependence between T_{SET} and *LET* for any $S_T > 1$ can be derived from the dependence between T_{SET} and *LET* for $S_T = 1$. The component $f(S_L, C_L)$ represents the contribution of the size factor of load gate at whose output the SET pulse width is determined, and the capacitance of interconnection wires and additional load gates (if fanout > 1). The $f(V_{DD})$ and $f(T_{EMP})$ components represent the increases or decrease of SET pulse width when V_{DD} and T_{EMP} increase or decrease with respect to the nominal values.

As an example to illustrate the modeling approach, the dependence between T_{SET} and LET, for an inverter with S_T =1 and low input level, is illustrated in Figure 4.20. Although this relation is logarithmic, when analyzed in semi-log scale (as shown in Figure 4.20), two regions can be observed: (i) a non-linear region for lower *LET*, and (ii) a linear region for higher *LET*. Considering the border points of each region, it is possible to identify three main points in Figure 4.20: LET_{TH} , LET_{DRIVE} and LET_{MAX} . LET_{TH} represents the threshold *LET*, while LET_{MAX} and LET_{DRIVE} are introduced to ease the model derivation. LET_{MAX} denotes the maximum value of *LET* considered during characterization, and it is chosen according to the target radiation

environment. In this case we have selected $LET_{MAX} = 60 \text{ MeV} \cdot \text{cm}^2 \cdot \text{mg}^{-1}$ since most particles encountered in space have lower *LET*. *LET*_{DRIVE} is the border point between the two regions, representing the value of *LET* for which the particle-induced current is equal to the target gate's driving current. The value of *LET*_{DRIVE} can be determined from current injection simulations. Thus, knowing the values of *LET*_{DRIVE}, *LET*_{TH} and *LET*_{MAX} allows to reconstruct the SET pulse width in terms of *LET*.

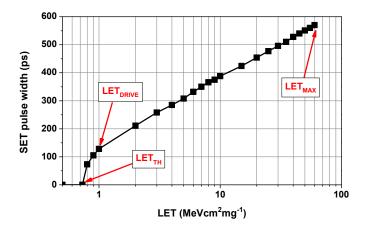


Figure 4.20: SET pulse width as a function of LET, for inverter with driving strength x1

According to the results depicted in Figure 4.20, the analytical expression for the SET pulse width T_{SET} as a function of *LET*, for a gate with minimum size factor $S_T = 1$, a single load gate with size factor $S_L = 1$, nominal supply voltage $V_{DD} = 1.2$ V and temperature $T_{EMP} = 27$ °C, can be formulated as [MA14, MA15],

$$f(LET, S_T = 1) = \begin{cases} b_0 + b_1 \cdot \ln(LET), & LET < LET_{DRIVE} \\ b_2 + b_3 \cdot \ln(LET), & LET \ge LET_{DRIVE} \end{cases}$$
(4.14)

Using relation (4.14), the logarithmic dependence of SET pulse width on *LET* can be approximated with two linear functions and four fitting coefficients (b_0 , b_1 , b_2 and b_3). The linear fitting functions are obtained by expressing the SET pulse width in terms of ln(*LET*), and then fitting the regions from *LET*_{TH} to *LET*_{DRIVE}, and from *LET*_{DRIVE} to *LET*_{MAX}. It is important to note that, for the sake of simplicity, the region *LET* < *LET*_{DRIVE} is approximated with a linear function despite the fact that it is non-linear (as can be observed in Figure 4.20).

The relation (4.14) is constructed for the minimum size factor of each gate. As demonstrated in Section 4.3.2, the SET pulse width decreases proportionally to the driving strength (size factor) of the target gate. Based on the simulation results for the investigate standard cell library, we have concluded that for any gate type, the SET pulse width T_{SET} for a given *LET* and size factor $S_T = n$ (where n > 1) can be obtained analytically from the T_{SET} values for $S_T = 1$, as follows [MA14, MA15],

$$f(LET, S_T = n) = f\left(\frac{LET}{n}, S_T = 1\right)$$
(4.15)

In order to accurately evaluate the impact of load settings, two aspects have to be considered. First, the SET pulse width increases with the increase of load size when *LET* is greater than LET_{DRIVE} , but decreases

with the increase of load size when *LET* is smaller than LET_{DRIVE} . Second, since the SET pulse width is analyzed at the output of a load gate, the model should consider the general case with an arbitrary number of load gates. Thus, the change (increase or decrease) of the SET pulse width with respect to the value obtained with relations (4.14) and (4.15) can be expressed as follows,

$$f(S_L, C_L) = \begin{cases} b_4 \cdot (S_L - 1) + b_5 \cdot C_L, & LET < LET_{DRIVE} \\ b_6 \cdot (S_L - 1) + b_7 \cdot C_L, & LET \ge LET_{DRIVE} \end{cases}$$
(4.16)

where the coefficients b_4 , b_5 , b_6 and b_7 are determined by linear fitting of the dependence between SET pulse width and load, as illustrated in Figure 4.11. For a general case with *K* load gates of different types, the relation (4.16) will have *K* different values for each fitting coefficient. If the SET pulse width is observed at the output of a target gate, only the total load capacitance would be relevant. Nevertheless, determining the SET pulse width at the output of load gates, rather than at the output of a target gate, is essential for simplifying the subsequent SET propagation analysis, because the SET pulse width model considers the propagation of an SET through one logic stage.

From the results presented in Section 4.3.2, the SET pulse width increases for a constant value ΔT_{SET_MAX} when V_{DD} increases from 1.2 to 1.32 V. Similarly, the SET pulse width decreases by almost equal value ΔT_{SET_MAX} when V_{DD} decreases from 1.2 to 1.08 V. Let's denote with ΔV_{DD_MAX} the maximum change of V_{DD} (e.g., $\Delta V_{DD_MAX} = 0.12$ V). Then, when V_{DD} increases or decreases by an arbitrary value ΔV_{DD} with respect to the nominal V_{DD} value, the change of SET pulse width can be expressed as,

$$f(V_{DD}) = b_8 \cdot \Delta V_{DD} = \frac{\Delta T_{SET_MAX}}{\Delta V_{DD_MAX}} \cdot \Delta V_{DD}$$
(4.17)

where ΔV_{DD} denotes the change of supply voltage with respect to nominal value (1.2 V), and b₈ is the fitting coefficient obtained by dividing the maximum SET pulse width change ΔT_{SET_MAX} and the corresponding maximum supply voltage change ΔV_{DD_MAX} .

As the impact of temperature is qualitatively similar to that of supply voltage, employing similar approach as defined by relation (4.17), the change of SET pulse width due to the change of temperature can be determined as,

$$f(T_{EMP}) = b_9 \cdot \Delta T_{EMP} = \frac{\Delta T_{SET_MAX}}{\Delta T_{EMP_MAX}} \cdot \Delta T_{EMP}$$
(4.18)

where ΔT_{EMP} denotes the change of temperature with respect to nominal value (27 °C), and b_9 is the fitting coefficient obtained by dividing the maximum change of SET pulse width ΔT_{SET_MAX} with the corresponding maximum temperature change ΔT_{EMP_MAX} .

Using relations (4.12) – (4.18), the generated SET pulse width in any node of a target circuit designed with the characterized cells can be determined as a function of the analyzed parameters, without additional simulations. A total of 12 model coefficients (*LET*_{TH}, *LET*_{DRIVE} and $b_0 - b_9$) are stored in a LUT for a given input level, one sensitive node in the target gate, one load gate type and one pair of timing constants of the current pulse.

To validate the proposed SET pulse width model, we have compared the results obtained with the model against those from SPICE simulations. A sample of results for different settings for INV, NAND2 and NOR2 gates is illustrated in Figure 4.21. The absolute error in predicting the SET pulse width is lower than 30 ps over the entire *LET* range up to 30 MeV·cm²·mg⁻¹. For *LET* values greater than 2 MeV·cm²·mg⁻¹, the relative error between the model and SPICE simulations is less than 10 %, which is consistent with the previously published models. However, for *LET* values below 2 MeV·cm²·mg⁻¹, the error goes up to 33 %, and that can be attributed to the fact that linear fitting for *LET* < *LET*_{DRIVE} was used in relation (4.14). Nevertheless, the higher relative error for low-LET values is not critical as very short SET pulses are less likely to propagate through the circuit.

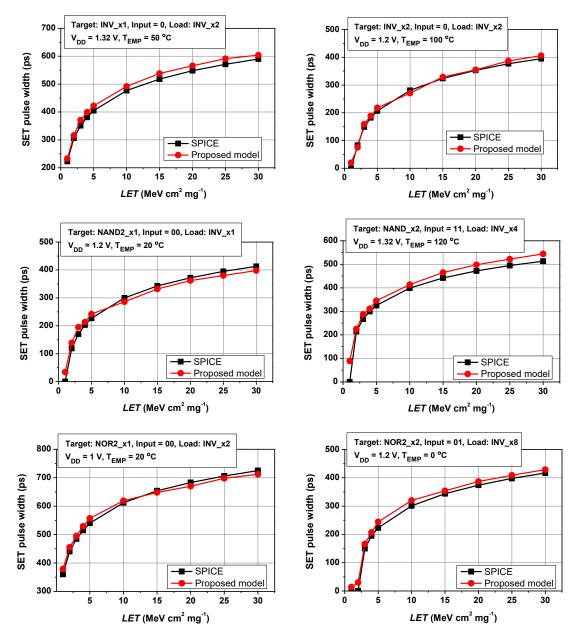


Figure 4.21: Comparison of generated SET pulse width from SPICE simulations and proposed model, for INV, NAND2 and NOR2 gates

The main benefit of the proposed SET pulse width model over previous models [220 - 224] is the use of bias-dependent SET current model, instead of the double-exponential current model. As a result, the proposed model provides a more accurate prediction of the SET pulse widths than the previous models. Furthermore, compared to the models [180, 227], which take into account the bias-dependence of the SET current, the superposition principle of the proposed model allows to assess individually the impact of different parameters. Similarly to the proposed critical charge model, this modeling approach can be easily applied to other technologies, because the individual relations constituting the model can be modified by applying alternative fitting functions, if required.

4.6.3 Propagated SET Pulse Width Model

To allow for analytical estimation of the SET pulse width variation due to propagation through a single logic gate, an SET propagation model is derived from the characterization results in Section 4.4. In the case when no logical masking occurs across the path, the SET propagation model enables to determine the pulse width at the output of a logic path (input of flip-flop) for a predefined SET pulse width at a particular circuit node. Consequently, the electrical and temporal masking factors can be determined.

It is important to note that the proposed model considers the variation of SET pulse width during propagation through a single gate, when the input pulse is sufficiently wide so that no significant attenuation can occur. In other words, the model considers the input pulses at least twice longer than the propagation delay of target gates, which is the most critical SET propagation scenario because such pulses can be significantly broadened during propagation through a logic path. On the other hand, as demonstrated in previous works [128, 228], the SET pulses shorter than the propagation delay will be filtered, while those wider than the propagation delay but shorter than twice of the propagation delay will be attenuated, and are not likely to reach the primary outputs of a logic circuit.

In contrast to previous SET propagation models elaborated in Section 3.3.4, we propose a model which does not express the propagated SET pulse width explicitly in terms of the propagation delay, but rather in terms of the parameters which define the propagation delay - size factor of target gate, load capacitance, supply voltage and temperature. Thus, the contribution of each parameter to the SET propagation can be assessed analytically. That is possible as the propagation delay is defined for each gate. To the best of our knowledge, none of the previously reported SET propagation models considers explicitly the impact of the aforementioned parameters. Moreover, none of the existing models takes into account the impact of temperature. It is important to consider the impact of supply voltage droop. This can significantly simplify and speed up the SET propagation analysis by eliminating the need to read the propagation delay for each gate from the library characterization (.LIB) file.

Based on the results in Section 4.4, we introduce an SET pulse propagation model by defining the pulse width at the output of a given logic gate, T_{OUT} , in terms of the input pulse width T_{IN} and propagation-induced pulse broadening/shrinking $\Delta \tau$ for a single gate. The broadening or shrinking is defined in terms of size factor of the gate S_T , total load capacitance C_L , supply voltage V_{DD} and temperature T_{EMP} . Note that unlike the critical charge and SET pulse width models where the load impact is divided in two contributions, because the SET response is observed at the output(s) of load gates, in the case of SET propagation model

the impact of load is represented with a total load capacitance, because the SET is observed at the output of target gate.

For each gate, the minimum input pulse width T_{IN_MIN} that can propagate through the gate without significant attenuation is initially determined from simulations. Note that the value of T_{IN_MIN} is determined by the propagation delay, i.e., it depends on gate type and size, as well as load capacitance, supply voltage and temperature. Thus, the propagation model for a given input pulse width $T_{IN} > 2T_{IN_MIN}$ can be expressed in a general form as,

$$T_{OUT} = T_{IN} \pm \Delta \tau = T_{IN} \pm c_0 \pm f(S_T, C_L, V_{DD}, T_{EMP})$$
(4.19)

As has been shown in Section 4.4, the variation of each parameter results in uniform increase or decrease of SET pulse width, depending on the input pulse polarity. This indicates that the SET pulse width model can be constructed employing a similar principle of superposition as that applied to the SET generation models. Thus, the propagation-induced pulse broadening/shrinking $\Delta \tau$ can be decomposed into multiple components, as follows,

$$\Delta \tau = \pm c_0 \pm f(S_T) \pm f(C_L) \pm f(V_{DD}) \pm f(T_{EMP})$$
(4.20)

In relation (4.20), the term c_0 denotes the initial change (broadening or shrinking) of the input pulse for nominal conditions, i.e. $\Delta \tau = \pm c_0$ for nominal conditions. The nominal conditions for the performed characterization are: $S_T = 1$ (minimum driving strength of a gate through which the SET propagates), $C_{L_NOMINAL} = 4.2$ fF (minimum load capacitance equivalent to a single load inverter with minimum driving strength), $V_{DD_NOMINAL} = 1.2$ V and $T_{EMP_NOMINAL} = 27$ °C. Therefore, a unique value of c_0 is assigned to every gate type. The \pm sign is used for each term because the propagated pulse width either increases or decreases, depending on the input pulse polarity.

The variation of propagated SET pulse width in terms of the size factor of target gate (i.e., for $S_T > 1$), while all other parameters are at nominal values, can be expressed with a power law,

$$f(S_T) = c_1 \cdot (S_T - 1)^{c_2} \tag{4.21}$$

where c_1 and c_2 are obtained by analytical fitting, as illustrated in Figure 4.16. The fitting coefficients c_1 and c_2 have unique values for each gate type.

The dependence of propagated SET pulse width on load capacitance is linear, and can be expressed as follows,

$$f(C_L) = c_3 \cdot S_T \cdot \left(C_L - C_{L_NOMINAL}\right) \tag{4.22}$$

where c_3 is the fitting coefficient, and the slope of this dependence is proportional to the size factor of target gate S_T , as shown in Figure 4.17.

The propagated SET pulse width may increase or decrease when the supply voltage decreases below the nominal value, according to the relation,

$$f(V_{DD}) = c_4 \cdot \left(V_{DD} - V_{DD \ NOMINAL}\right)^{c_5}$$
(4.23)

where c_4 and c_5 are determined by employing a power law to fit the simulated dependence between the change of SET pulse width and the change of supply voltage.

The change of propagated SET pulse width as a result of increase or decrease of temperature beyond the nominal value can be expressed as follows,

$$f(T_{EMP}) = c_6 \cdot \left(T_{EMP} - T_{EMP_NOMINAL}\right)$$
(4.24)

where c_6 is obtained by linear fitting of dependence between the change of propagated SET pulse width and the change of temperature. Since the change of propagated SET pulse width is similar for the same increase or decrease of temperature beyond $T_{EMP_NOMINAL} = 27$ °C, a single fitting coefficient is used.

Note that the impact of supply voltage and temperature slightly varies with the size factor of target gate S_T and total load capacitance C_L . However, this dependence was neglected in order to simplify the model, without significantly affecting the accuracy. For better accuracy, the relations (4.23) and (4.24) can be extended to take into account the impact of S_T and C_L .

Therefore, based on relations (4.19) - (4.24), the SET pulse width at the output of a logic gate can be determined as a function of input pulse width and four parameters considered in the characterization (size of target gate, load capacitance, supply voltage and temperature). For each gate type, 7 model coefficients are obtained: $c_0 - c_6$. Note that the model coefficients are obtained for a given input pin, but not for the input logic levels as in the case of critical charge and generated SET pulse width models. The model coefficients are stored with the respective sign (positive or negative) for one input level, and for the opposite input level the sign is only reversed, without the need to use additional LUT. As a result, one LUT is sufficient to store all model coefficients for a given gate type. Besides the LUTs with model coefficients, it is also necessary to store in separate LUTs the values of T_{IN-MIN} for all investigated conditions.

To verify the proposed model, four characteristic logic paths (Table 4.19) have been chosen, and the output pulse width was determined from SPICE simulations and with the proposed model. All paths consist of less than 15 gates, as this is a typical logic path length in modern designs. Moreover, as demonstrated in Section 4.4, the shrinking or broadening across short paths can be significant, and it is thus important to consider such scenarios. Path 1 is composed solely of inverters, thus resembling the typical paths in clock trees. Path 2 is composed only of NAND and NOR gates, as most logic functions can be implemented with these two gates. Paths 3 and 4 consist of different types of gates, which is common in complex logic circuit. The paths are composed of logic gates with driving strengths x1 and x2. Note the critical paths in a real design may be longer. However, as any combinational circuit can be partitioned into multiple smaller circuits, the logic paths can be also regarded as multiple connected paths. Instead of propagating a trapezoidal pulse through the path, a bias-dependent current source was used to generate a realistic SET

pulse at the output of first gate, and the resulting pulse width was observed at the path output. The width of the induced SET was determined from simulations and then used as input for the proposed model to calculate the output SET pulse width. This approach was chosen in order to give a more realistic view of the accuracy of the model proposed in predicting the SET pulse width. The induced current pulse with LET = $10 \text{ MeVcm}^2\text{mg}^{-1}$ was used in all simulations.

The SET pulse widths at the outputs of investigated paths, obtained from SPICE simulations and with the proposed model, are given in Table 4.20. It can be seen that the relative error of the model is less than 12 % for all investigated cases. The relative error is larger when initial SET pulse is shorter, e.g., for investigated paths the largest error was obtained for SET pulse widths shorter than 400 ps. This is reasonable because the relative error per gate is uniform over the investigated pulse width range. Overall, the proposed model has a very good accuracy in predicting both propagation-induced broadening and shrinking across homogeneous and heterogeneous logic paths.

Path notation	Path composition (from input to output)
Path 1 (10 gates)	$\begin{array}{l} INV_x1-INV_x2-INV_x4-INV_x1-INV_x4-INV_x2-\\ INV_x1-INV_x1-INV_x2-INV_x2\end{array}$
Path 2 (6 gates)	NAND2_x1 - NOR2_x1 - NOR2_x2 - NAND2_x2 - NAND2_x1 - NOR2_x2
Path 3 (10 gates)	AND2_x1 - NOR2_x1 - AND2_x1 - OR2_x2 - INV_x1 - AND2_x2 - OR2_x1 - INV_x1 - AND2_x1 - NAND2_x1
Path 4 (12 gates)	NOR3_x1 - AND2_x2 - NAND4_x1 - INV_x2 - XOR2_x1 - AND4_x1 - OR3_x1 - NAND2_x1 - NOR2_x1 - INV_x2 - OR4_x1 - XNOR2_x1

Table 4.19: Description of combinational paths used for model verification

Table 4.20: Comparison of SET propagation through combinational paths from Table 4.19, with proposed model and SPICE simulations, when the current pulse with $LET = 10 \text{ MeV cm}^2\text{mg}^{-1}$ is injected in the output of first gate in each path

Simulation conditions	Pulse width at first node (ps)	Output pulse width from SPICE (ps)	Output pulse width from model (ps)	Relative error (%)
Path 1, $V_{DD} = 1.20$ V, $T_{EMP} = 30$ °C	333	368	411	11.7
Path 1, $V_{DD} = 1.00$ V, $T_{EMP} = 50$ °C	393	445	479	7.6
Path 2, $V_{DD} = 1.20$ V, $T_{EMP} = 100$ °C	401	455	424	4.6
Path 2, $V_{DD} = 1.08$ V, $T_{EMP} = -10$ °C	419	483	451	3.7
Path 3, $V_{DD} = 1.20$ V, $T_{EMP} = 40$ °C	380	358	388	8.4
Path 3, $V_{DD} = 1.00$ V, $T_{EMP} = 125$ °C	445	407	382	6.1
Path 4, V_{DD} = 1.20 V, T_{EMP} = -20 °C	544	711	744	4.6
Path 4, $V_{DD} = 1.08$ V, $T_{EMP} = 80$ °C	596	840	876	4.3

4.7 SET Effects in Application-Specific Standard Cells

Although digital designs are predominantly composed of standard cells, it is often necessary to extend the library with the custom-designed cells in order to achieve additional functionality that is not supported by the existing standard cells. To investigate the SET effects and the applicability of the derived SET models to application-specific standard cells, the analysis was conducted for two cells commonly used in rad-hard designs: a Muller C-element and a Single Event Latchup (SEL) protection switch.

4.7.1 SET and SEU Effects in a Muller-C Element

A Muller C-element, originally designed by David Muller [286], is a fundamental building block of asynchronous circuits. It is essentially a hybrid of an AND gate and a state-holding element. When the inputs are equal, the output is equivalent to the inputs. Otherwise, when the inputs differ, the output retains the previous state. Therefore, the C-element is potentially sensitive to both SETs and SEUs. Given that a large part of any asynchronous design may be occupied by C-elements, the analysis of their sensitivity to SET and SEU effects is essential in the design of robust asynchronous systems. While the SET and SEU effects in C-elements have been thoroughly addressed, to the best of our knowledge, **there is no a known report on analytical SET/SEU sensitivity model applicable to C-element**.

In this work, we have investigated the Van Berkel's C-element implementation [287]. The schematic of Van Berkel's C-element and the C-element truth table are shown in Figure 4.22. Using the same simulation setup as for standard cells analyzed in previous sections, the critical charge for SET and SEU at the output node has been analyzed for IHP's 130 nm and UMC's 65 nm CMOS technologies [MA9]. The analysis was done for two conditions: (i) for SET – both inputs are at high level, and (ii) for SEU – both inputs are initially at high level and then input A changes to low level. The double-exponential current pulse with the rise time of 10 ps and the fall time of 50 ps was injected in the output of the element. To achieve realistic operating conditions, an inverter was used as a load. The simulations have been done for different sizes of C-element and load inverter, and for the same range of supply voltage and temperature as for the standard cells. The minimum W/L ratio for all PMOS transistors was 810nm/130nm for 130 nm technology, and 500nm/80nm for 65 nm technology. We denote the minimum W/L ratio as the minimum driving strength x1. The PMOS-to-NMOS ratio was 2 for all transistors in the cell. Upsizing was accomplished by increasing the channel width of all transistors. Note that both investigated technologies operate with the nominal supply voltage of 1.2 V.

Figure 4.23 illustrates the dependence of the SET and SEU critical charge on the size factor of Celement, for the minimum-sized load inverter, nominal supply voltage of 1.2 V, and temperature of 27 °C. The SET critical charge for 65 nm technology is approximately twice lower than for 130 nm technology, which is expected since the reduction of feature size leads to a decrease of critical charge. Similar trend can observed for the SEU critical charge. It can be noticed that the critical charge for SEU is slightly larger than that for SET, for both technologies. That is reasonable, as the SEU represents a full swing of the voltage level, and thus more charge is required to cause an SEU than an SET. The upsizing of C-element results in a linear increase of the critical charge, for the investigated size factors up to x8. This is in good agreement with the results obtained for standard cells. By doubling the C-element's size, the critical charge for both SET and SEU increases by approximately 100 %.

Output Z

0

1

0

1

0

1

The analysis was also conducted for different load size, supply voltage and temperature. Since the qualitative dependence of critical charge on these parameters is very similar to that for the standard cells presented in Section 4.3.1, the respective graphs are not shown here. The impact of the size of load inverter is significantly weaker compared to the C-element size. Namely, the critical charge of the output node of C-element increases by less than 10 % when the size of load inverter is doubled. The supply voltage variation plays a significant role, as the change of supply voltage by \pm 10 % results in an increase or decrease of the critical charge by approximately 20 %. The impact of temperature variation is moderate, as the critical charge varies by a maximum of 10 % over the temperature range from -40 to 125 °C. Similarly to the SET response, the dependence between the critical charge for SEU and the analyzed parameters was almost linear for all investigated cases (with exception of temperature where slight non-linearity was observed). Moreover, the relative contribution of each investigated parameter to the SEU critical charge was similar as in the case of SET.

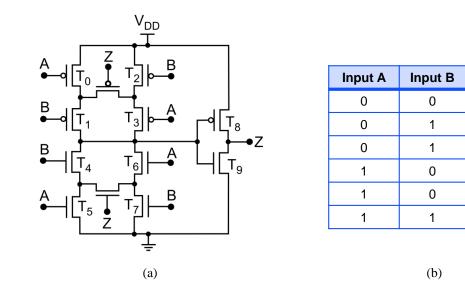


Figure 4.22: (a) Van Berkel's C-element, and (b) C-element truth table

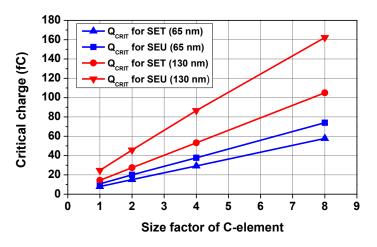


Figure 4.23: Comparison of SET and SEU critical charge as a function of size factor of C-element, for INV_x1 as a load, and nominal supply voltage and temperature

To investigate the possibility of using the proposed critical charge model for analysis of C-element, the fitting procedure introduced in Section 4.6.1 has been applied to derive the model coefficients. In this case, four parameters have been considered – size factor of C-element (S_T), size factor of load inverter (S_L), supply voltage (V_{DD}) and temperature (T_{EMP}). The accuracy of the model was assessed in terms of the relative difference between the values determined with the SPICE simulations and with the derived model, and the obtained results are presented in Table 4.21. In all cases the relative difference was lower than 11 %. These relative errors are within the range obtained for standard cells, confirming very good accuracy of the model. The highest relative errors were obtained for certain corner values of supply voltage and temperature. Such errors are due to the applied approximations in the model derivation, i.e., slight nonlinearities have been modeled as linear dependencies.

Simulation conditions			ditions	Q _{CRIT} for 130 nm (fC)			Q _{CRIT} for 65 nm (fC)		
S_T	S_L	V _{DD} (V)	<i>Т_{ЕМР}</i> (°С)	SPICE	Model	Relative error (%)	SPICE	Model	Relative error (%)
1	2	1.2	27	14.3	13.2	7.7	8.2	7.75	5.5
2	3	1.32	125	35.9	33.42	6.9	18.44	17.29	6.2
4	5	1.08	-40	52.4	51.1	2.5	26.96	25.65	4.9
8	7	1.2	125	113.4	107	5.6	55.52	54.46	1.9
1	7	1.32	-40	30.9	30.31	1.9	13.72	12.95	5.6
2	5	1.08	27	29.5	27.66	6.2	14.04	12.85	8.5
4	3	1.2	-40	60	59.2	1.3	32.68	31.63	3.2
8	1	1.32	27	127	126	0.6	71.8	70.9	1.3
1	1	1.08	125	11.5	10.4	9.6	5.72	5.12	10.5

Table 4.21: Comparison of critical charge obtained with proposed model and SPICE simulations for C-element designed in 130 and 65 nm technologies

4.7.2 SET Effects in a SEL Protection Switch

Despite the fact that technological advancement has rendered modern CMOS technologies highly robust to hard SEEs, the SEL can still occur in some advanced technologies (e.g., FinFET) [288], as well as in some digital circuits (e.g., SRAMs) [289]. The SEL is a type of hard SEE caused when an energetic particle triggers the parasitic thyristor (PNPN) structure inherent in CMOS technologies. Besides, the SEL can be triggered by the electrostatic discharge and supply noise. It is manifested as an abrupt increase of supply current, which can damage the circuit if the power is not restarted. In highly scaled technologies, the micro SELs (micro latchups) occurring in localized regions in the circuit, and resulting in the increase of supply current in discrete steps, may be a serious issue [289]. For that reason, the SEL protection measures may need to be considered for many rad-hard designs intended for harsh radiation environments such as space. A common SEL protection approach is based on detection of excessive supply current flow, and subsequent resetting of the power supply to restore the normal operation. Nevertheless, the SEL protection circuitry may be sensitive to SETs and this should be addressed during the design process.

In this work, we have investigated the SET sensitivity of a SEL Protection Switch (SPS cell) proposed by Petrovic *et al.* [290]. Figure 4.24 shows the block-diagram of the SPS cell and its interface to the on-

chip circuitry. The SPS cell provides the on-chip SEL protection of standard cells. It has been designed in IHP's 130 and 250 nm technologies, and its functionality has been verified through both simulations and irradiation experiments [290]. A detailed description of the design and operation of the SPS cell can be found in [290]. The SPS cells are distributed across the chip, such that one SPS cell can protect tens or hundreds of standard cells. In a complex design, thousands of SPS cells may be required. The analysis of SET effects in the SPS cell is particularly interesting due to its unique design, and also because of its unique interface (it is connected to the power supply terminals of standard cells).

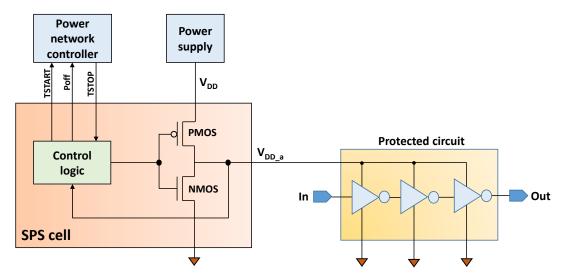


Figure 4.24: SPS interface with external logic

The SPS design is based on the use of a large PMOS transistor which serves as a current sensor/driver, originally proposed by Nicolaidis [291]. The PMOS sensing/driving transistor delivers the power supply to the standard cells and detects the excessive current flow, while the complementary NMOS transistor acts as a discharger. The rest of the circuit, denoted as Control logic in Figure 4.24, consists of 11 transistors for controlling the operation of the PMOS sensing/driving transistor and interfacing with the external circuitry. In the normal mode of operation, the power supply is fed to the standard cells via the V_{DD_a} line, i.e., $V_{DD_a} = V_{DD}$. In the case of excessive current flow through the PMOS transistor, the voltage across the V_{DD_a} node falls. If the V_{DD_a} falls below the threshold level ($V_{DD}/2$), the control logic will change the state of the TSTART signal to inform the Power network controller that SEL has occurred. As a response to SEL, the Power network controller activates the Poff signal to shut down the power supply to the standard cells. After a predefined time interval, the Power network controller deactivates the Poff signal and sets the TSTOP input to restore the power supply. As the SPS cell is a combinational circuit, the SETs may have two adverse effects: (i) cause a false SEL indication on TSTART node, and (ii) disrupt the power supply delivered to the standard cells.

To investigate the SET effects in the SPS cell, we have conducted extensive simulations for 130 nm and 250 nm technologies, considering the impact of PMOS sensing/driving transistor's size ratio W/L, number of load inverters N connected to V_{DD_a} , and width of the double-exponential current pulse T_{PULSE} defined as the difference between the fall time constant and the rise time constant [MA1, MA4, MA5]. The same

simulation setup as in previous discussion was used to inject the current in the V_{DD_a} node. The rise time constant of the double-exponential current pulse was 10 ps. As the SPS cell is intended to operate with fixed supply voltage, all simulations have been conducted for the nominal supply voltage. Note that the nominal supply voltage is 1.2 V for 130 nm technology, and 2.5 V for 250 nm technology.

Figure 4.25 depicts the dependence of critical charge on W/L ratio of PMOS transistor and number of load inverters N, for $T_{PULSE} = 100$ ps. The critical charge increases linearly with the increase of both W/L and N. The simulations have also confirmed that the critical charge increases linearly with T_{PULSE} . It can be seen that the 130 nm SPS cell has lower critical charge than the 250 nm design, as expected. The increase of the number of inverters is less effective for improving the SET robustness in the case of 130 nm technology, and this may be due to the fact that the inverters in 130 nm technology have smaller dimensions, and therefore smaller capacitance, than the equivalent inverters designed in 250 nm technology.

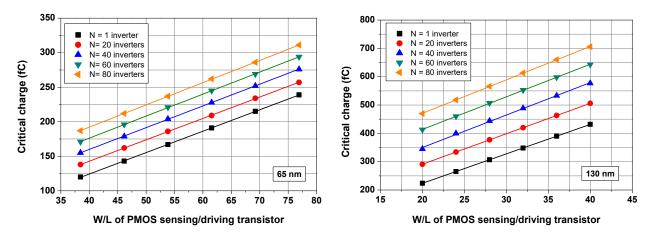


Figure 4.25: Critical charge of the output node of SPS cell as a function of *W/L* ratio of PMOS sensing/driving transistor and number of load inverters *N* (for fixed supply voltage, temperature and timing parameters of current pulse)

By comparing the presented results with those obtained for standard cells in Section 4.3.1, two main differences can be observed. First, due to large transistor sizes, the SPS cell is more robust to SETs than the standard cells. For example, with the minimum sized PMOS transistor the critical charge is already beyond 100 fC, whereas all standard cells with the minimum driving strength have critical charge lower than 100 fC. Second, the impact of load on the SET robustness of SPS cell is stronger than in the case of standard cells, and this is due to different interfacing (supply terminals of standard cells act as load for SPS cell, as depicted in Figure 4.23). It can be seen in Figure 4.25 that increasing the number of load gates may result in higher critical charge than increasing the *W/L* ratio of sensing/driving transistor.

Depending on the transistor sizing of the SPS cell for a particular design, it may be required to enhance its SET robustness. That could be achieved by combination of the upsizing of sensing/driving transistor and increasing the number of load gates. To facilitate fast estimation of the SPS cells' SET robustness, we have analyzed the applicability of the critical charge model defined in Section 4.6.1. Due to different design, the critical charge model has been slightly modified to incorporate the parameters analyzed in this case. Thus, the model expressing the critical charge of the output node of SPS cell in terms of *W/L* ratio of sensing driving transistor, number of load inverters N and current pulse width T_{PULSE} , where the minimum current pulse width is $T_{PULSE_MIN} = 100$ ps, can be expressed as [MA1, MA4, MA5],

$$Q_{CRIT} = a \cdot \frac{W}{L} + b \cdot N + c \cdot \frac{W}{L} \left(T_{PULSE} - T_{PULSE_{MIN}} \right)$$
(4.25)

In order to verify the critical charge model defined by the relation (4.25), the relative differences between the critical charge values obtained with the SPICE simulations and with the model have been calculated for both technologies. The analysis was done for all combinations of five values of W and N, and four values of T_{PULSE} . The results for ten selected combinations are given in Table 4.22. For all investigated cases the relative difference was lower than 6.5 %. These results confirm that the proposed critical charge model is convenient for evaluation of the SET robustness of the SPS cell.

Table 4.22: Comparison of critical charge obtained with proposed model and SPICE simulations for SEL protection switch designed in 130 and 250 nm technologies

Simulation conditions			Q _{CRIT} for 130 nm (fC)			Q _{CRIT} for 250 nm (fC)		
W (µm)	N	T _{PULSE} (ps)	SPICE	Model	Relative error (%)	SPICE	Model	Relative error (%)
5	1	100	224	222.93	0.48	120	120.53	0.44
6	20	100	334	330.22	1.13	162	161.58	0.26
7	40	100	444	440.84	0.71	204	203.46	0.26
8	60	400	1344	1271.8	5.37	702	668.1	4.83
9	80	400	1572	1472.5	6.33	806	762.2	5.43
9	1	700	1907	2018.6	5.85	1153	1173.8	1.8
8	20	700	1838	1858.2	1.1	1065	1059.1	0.55
7	40	1000	2334	2331	0.13	1319	1316.5	0.19
6	60	1000	2127	2083.9	2.03	1168	1150.7	1.48
5	80	1000	1902	1836.8	3.43	1012	1072.4	5.97

4.8 Optimization of SET Characterization Process

The results presented in previous sections have shown that the characterization of SET effects in a standard library is an exhaustive process which requires to consider multiple dependencies between the SET sensitivity metrics and the contributing parameters. In other words, a large number of simulations are needed to analyze all possible combinations of parameters, and the resulting database requires a large number of LUTs to store all the data. The application of such extensive SET database could be a bottleneck in the analysis of a particular circuit, due to the time required to read the LUT contents. In addition, the storage of a large database often requires considerable memory space. Thus, there is a strong need to optimize the overall SET characterization process by: (i) reducing the number of simulations during characterization, and (ii) reducing the number of values in the SET database. Based on the conducted analysis, we propose an approach to reduce both the number of simulations and the size of output SET database.

4.8.1 Reduction of Number of Simulations

In state-of-the-art SET characterization approaches, the simulations are performed for all nodes within each gate and all combinations of parameters affecting the SET sensitivity. Although this is done only once for a given library, it may be very exhaustive since modern digital libraries may contain hundreds or even thousands of standard cells. Furthermore, the standard libraries may be upgraded with new standard cells or custom-designed rad-hard cells that also have to be characterized. Besides the characterization of standard cells, the gate-level hardening solutions have to be characterized as well, which is usually not considered in the existing approaches. Then, the complete procedure would have to be repeated for every new technology, which would significantly slow down the transition to a new generation or evaluation of a new technology for a particular application. All aforementioned factors impose the need to optimize the characterization process by reducing the number of required simulation runs.

A well-known approach for optimization of SET characterization is based on the use of equivalent inverters, i.e. all logic gates with multiple inputs are represented with equivalent inverters, where the equivalence is defined by the transistors' channel resistance (channel resistance is inversely proportional to channel width). Subsequently, the simulations are done only for different design and operating settings for equivalent inverters. This concept was applied for critical charge characterization [219] and SET pulse width characterization [180]. However, this approach is not sufficiently accurate for complex logic gates which have multiple SET sensitivity levels, as opposed to inverters with only two sensitivity levels. Another widely used approach to optimize the characterization process is by performing the simulations only for the output nodes of each gate. However, this approach may compromise the accuracy, as some internal nodes may be actually more sensitive than the output node. Alternatively, the pruning techniques [183] can be applied to reduce the number of simulation points (e.g. conducting simulations for the minimum number of points required to capture the relevant effects). However, the pruning requires additional analysis efforts and may be required to apply different pruning techniques for different data sets.

Based on the results presented in Section 4.4.4, the number of required simulations can be reduced by leveraging some inherent features of the gates' SET response. Specifically, the number of simulations can be reduced by exploiting the fact that **for multi-input gates, several input levels may have the same SET sensitivity**. As has been demonstrated in Section 4.3.1, for 3- and 4-input gates it is sufficient to perform the simulations only for a subset of input levels due to similarities in the SET sensitivity (critical charge and generated SET pulses width). This can significantly reduce the number of simulations for 3- and 4-input gates which have the largest number of input vectors. It is important to note that the reduction of simulations based on similarity in SET response for different input levels is applicable only for the SET generation analysis. Nevertheless, as most of simulations are done for SET generation characterization, the savings in the number of simulation runs during critical charge and generated SET pulse width analysis would be very beneficial for optimizing the overall characterization process.

The possible reduction in the number of simulations can be quantified mathematically. Lets consider a general case of characterization of critical charge for an arbitrary target gate with *P* inputs, i.e., 2^{P} input levels/vectors. The critical charge has to be characterized in terms of five parameters, where for each parameter a predefined number of values has to be considered, as follows: (i) number of different drive strengths of target gate N_{T} , (ii) number of different driving strengths of a load gate N_{L} , (iii) number of

different supply voltages N_{VDD} , (iv) number of different temperatures N_{TEMP} , and (v) number of different interconnection capacitances N_{W} . For the sake of simplicity, let's assume that only one sensitive node (e.g. output node) is analyzed. If a target gate is characterized for all combinations of aforementioned five parameters, and all input vectors, the total number of simulation values would be,

$$N_{TOTAL_SIM_STANDARD} = 2^P \cdot N = 2^P \cdot \prod_{i=1}^5 N_i, \tag{4.26}$$

where N_i denotes the number of different values for each of the analyzed parameter, i.e., $N_1 = N_T$, $N_2 = N_L$, $N_3 = N_{VDD}$, $N_4 = N_{TEMP}$, and $N_5 = N_W$. The product of the number of all five contributing parameters is denoted as N. For example, if four values are considered for each parameter, then N = 1024, i.e., 1024 simulation runs have to be performed.

The number of simulations for multi-input gates can be reduced if the simulations are not repeated for those input levels which yield the same or very close results. Hence, the total number of simulations with optimized approach is obtained by modifying relation (4.26) as follows,

$$N_{TOTAL_SIM_OPTIMIZED} = (2^{P} - L) \times N = (2^{P} - L) \times \prod_{i=1}^{5} N_{i}, \qquad (4.27)$$

where *L* is the number of input levels for which the simulations do not have to be repeated. For example, according to the results in Section 4.3.1, for NAND3 gate the simulations can be performed for 4 instead of 8 input levels, while for NAND4 the simulations can be performed for 5 instead of 16 input levels. Thus, L = 4 for NAND2, and L = 11 for NAND4.

Employing equations (4.26) and (4.27), the number of required simulations for standard and optimized characterization approaches is computed as given in Table 4.23. For generality, the number of simulations is expressed in terms of. *N*. As can be observed, by leveraging the inherent similarities in the SET sensitivity for different input levels, the number of required simulation runs for characterization of 18 standard logic gates can be reduced by 48 %, considering only the similarities in the SET sensitivity for multiple input levels of 3- and 4-input gates. For INV and BUF it is not possible to reduce the number of simulations with the proposed approach because theses gates have only one input. Although the results in Section 4.3.1 have shown that the critical charge for 2-input gates can be very close for 2 or 3 input levels, in this cases we have considered only the reduction of simulations for 3- and 4-input gates because they have the largest number of possible input vectors. Note that the proposed method for reduction of the number of simulations is applicable to standard cells with uniform transistor sizing. In the case of custom-designed cells, the dependence of SET sensitivity on input levels would have to be re-evaluated. It is also important to emphasize that the reduction of simulations with the proposed approach comes at the expense of less than 5 % error because of slight difference in the values of critical charge and generated SET pulse width for input levels that are considered as equivalent.

The total simulation time for characterization of all standard cells in a given library depends on the number of cells/gates, number of simulation runs (number of parameter values), and simulation time for

one run. In general, as the simulation setup is the same for all cells, the simulation time required to characterize one gate is roughly equal to the product of number of simulation runs and simulation time for one run. For simplicity of analysis, in this section we have considered only 4 values for each parameter, but in real characterization that number would be larger. In addition, the simulation time also depends on the automation process which is employed to run the simulations. As the automation of simulations is beyond the scope of this work, we have not analyzed the impact of different automation algorithms on the total simulation time.

	No. of simu	**
Gate type	Standard characterization	Optimized characterization
INV	$2 \cdot N$	$2 \cdot N$
BUF	$4 \cdot N$	$4 \cdot N$
AND2	$4 \cdot N$	$4 \cdot N$
AND3	$8 \cdot N$	4N
AND4	16·N	$5 \cdot N$
NAND2	$4 \cdot N$	$4 \cdot N$
NAND3	$8 \cdot N$	$4 \cdot N$
NAND4	16·N	$5 \cdot N$
OR2	$4 \cdot N$	$4 \cdot N$
OR3	$8 \cdot N$	$4 \cdot N$
OR4	16·N	$5 \cdot N$
NOR2	$4 \cdot N$	$4 \cdot N$
NOR3	$8 \cdot N$	$4 \cdot N$
NOR4	16·N	$5 \cdot N$
XOR2	$4 \cdot N$	$4 \cdot N$
XOR3	$8 \cdot N$	$4 \cdot N$
XNOR2	$4 \cdot N$	$4 \cdot N$
XNOR3	8·N	$4 \cdot N$
Total number of simulations	142·N	74·N

Table 4.23: Number of simulation runs for characterization of SET generation sensitivity of standard logic cells, for standard and optimized characterization approaches

4.8.2 Reduction of SET Sensitivity Database

The number of values obtained from simulation-based characterization is equivalent to the number of simulations, according to the relations (4.26) and (4.27). This number can range from tens to hundreds of thousands, even for optimized characterization. In other words, the characterization database for the SET sensitivity of entire standard cell library would require hundreds or thousands of 2D LUTs to store all values, where each LUTs stores the values for two parameters. Using the SET sensitivity models derived from the simulation data, the total number of characterization results can be reduced to form an optimized SET sensitivity database – a model-based SET sensitivity database. The idea of the proposed approach is

to store the models coefficients in 2D LUTs instead of raw simulations data, thus reducing significantly the total amount of stored data. As a result, the memory required to store the SET sensitivity database can be reduced significantly, and the subsequent SER analysis can be performed faster because significantly less amount of data would have to be read during the analysis.

Initially, the simulation results for each cell type are stored in 2D LUTs. The number of LUTs and the number of elements per LUT depend on the number of characterization parameters. For each cell type, three sets of LUTs have to be constructed: (i) critical charge LUTs for storing the critical charge values in terms of analyzed parameters, (ii) SET pulse width LUTs for storing the generated SET pulse widths in terms of analyzed parameters, and (iii) SET propagation LUTs for storing the propagated SET pulse width in terms of analyzed parameters. Note that the contributing parameters for SET sensitivity metrics may differ (e.g., input pulse width is considered only for SET propagation analysis, and LET is considered only for generated SET pulse width analysis).

As an example, a generic structure of 2D LUTs for storing the critical charge values obtained from simulations is illustrated in Figure 4.26. The LUTs store the critical charge in terms of 3 parameters (size factor of target gate S_T , size factor of load gate S_L and supply voltage V_{DD}). For each parameter, 4 different values are considered. Thus, four LUTs are obtained, where each LUT consists of 16 values, with a total of 64 values. When the characterization is performed for additional parameters, the 4 LUTs shown in Figure 4.26 have to be constructed for each combination of additional parameters.

L	UT4	$Q_{CRIT} (S_{T'} S_L)$ for V_{DD4}					
LU	ТЗ		Q _{CRIT} (S _T , S _L)) for V _{DD3}			
LUT	2	С	R _{CRIT} (S _T , S _L) 1	for V _{DD2}			
LUT1		$Q_{CRIT} (S_T, S_L)$ for V_{DD1}					
		S _L =1	S _L =2	S _L =4	S _L =8		
	S _T =1	Q _{CRIT} (1,1)	Q _{CRIT} (1,2)	Q _{CRIT} (1,4)	Q _{CRIT} (1,8)		
	S _T =2	Q _{CRIT} (2,1)	Q _{CRIT} (2,2)	Q _{CRIT} (2,4)	Q _{CRIT} (2,8)		
	S _T =4	Q _{CRIT} (4,1)	Q _{CRIT} (4,2)	Q _{CRIT} (4,4)	Q _{CRIT} (4,8)		
	S _T =8	Q _{CRIT} (8,1)	Q _{CRIT} (8,2)	Q _{CRIT} (8,4)	Q _{CRIT} (8,8)		

Figure 4.26: A generic example of four LUTs for storing the critical charge values in terms of size factor of target gate, size factor of load gate and supply voltage, for nominal values of all other parameters (for a single input vector, one sensitive node and fixed timing parameters of current pulse)

In Table 4.24, an example for the critical charge LUTs, showing the increase of the number of LUTs and total characterization values when the number of characterization parameters increases, is shown. For the sake of simplicity, five parameters are considered, for a single node in one target gate, one type of load gate, one input level/vector and fixed timing parameters of current pulse. With these conditions, a total of 64 LUTs (containing 1024 values) are required. The number of LUTs and total values will increase when

all relevant input levels are taken into account. Thus, 2×64 LUTs for 1-input gates and 4×64 LUTs for 2-inputs gates are required for critical charge. For 3-input gates, 4 input vectors have to be considered for optimized characterization, according to Table 4.25. Similarly, for 4-input gates, 5 input vectors have to be considered. Therefore, for 3- and 4- input gates, 4×64 and 5×64 LUTs have to be considered, respectively. The number of LUTs will increase further when additional parameters are included. For generated SET pulse width the number of LUTs is similar. In the case of propagated SET pulse width, the number of LUTs is defined by the number of inputs for each gate, and not by the number of input vectors.

Build-up of critical charge LUTs	No. of LUTs	No. of elements
$Q_{CRIT} = f(S_T, S_L)$	1	16
$Q_{CRIT} = f(S_T, S_L, V_{DD})$	4	64
$Q_{CRIT} = f(S_T, S_L, V_{DD}, T_{EMP})$	16	256
$Q_{CRIT} = f(S_T, S_L, V_{DD}, T_{EMP}, C_W)$	64	1024
$Q_{CRIT} = f(S_T, S_L, V_{DD}, T_{EMP}, C_W, Input_levels)$	$64 \cdot (2^{P} - L)$	$1024 \cdot (2^{P} - L)$

Table 4.24: Number of LUTs and elements in LUTs for storing the critical charge values for one gate type, obtained from standard characterization

By establishing analytical models from simulation data, and then storing the model coefficients in LUTs, both the number of LUTs and the total number of stored values can be reduced. As the proposed models are based on superposition principle, by increasing the number of parameters considered in analysis, the model coefficients will increase linearly. For instance, the critical charge in terms of drive strength, for all other parameters at nominal values, will be a linear function with three fitting coefficients. If the critical charge is expressed in terms of drive strength and load size, the total number of coefficients will increase to six. Thus, the total number of fitting coefficients of the model can be expressed as,

$$N_{TOTAL_MODEL} = (2^P - L) \times \sum_{i=1}^{6} M_i$$
 (4.28)

Comparing the equations (4.27) and (4.28) reveals that, for the same number of parameters, the equation (4.28) will result in significantly smaller number of values due to the summation of model coefficients, while in equation (4.27) the number of parameters are multiplied, resulting in significantly larger number. This shows that the proposed concept of storing the model coefficients in LUTs instead of raw simulation data can significantly reduce the number of characterization values. The 2D LUTs for storing the model coefficients are constructed such that each LUT stores the model coefficients for all relevant input levels, for a single sensitive node and a single pair of timing parameters of the current pulse.

In Figures 4.27 – 4.29, generic structures of the model-based 2D LUTs for storing the fitting coefficients for three SET sensitivity models (critical charge, generated SET pulse width and propagated SET pulse width) are shown. For critical charge and generated SET pulse width models, the model coefficients for all inputs levels are stored. Note that the values are stored for the optimized number of input levels 2^{P} – L. For propagated SET pulse width, the model coefficients for all input pins are stored.

	Critical charge model LUT					
	Input 1	Input 2		Input 2 ^P - L		
Q _{NOM}	Q _{NOM} (1)	Q _{NOM} (2)		Q _{NOM} (2 [₽] -L)		
a _0	a ₀ (1)	a ₀ (2)		a ₀ (2 ^P -L)		
a 1	a1(1)	a1(2)		a1(2 ^P -L)		
a ₂	a2(1)	a2(2)		a₂(2 [₽] -L)		
a 3	a ₃ (1)	a ₃ (2)		a₃(2 [₽] -L)		
a ₄	a ₄ (1)	a4(2)		a₄(2 [₽] -L)		
a ₅	a ₅ (1)	a ₅ (2)		a₅(2 [₽] -L)		
a ₆	a ₆ (1)	a ₆ (2)		a ₆ (2 [₽] -L)		

Figure 4.27 A generic 2D LUT for storing the coefficients for critical charge model, for a particular gate and all input vectors (for one sensitive node in target gate, and fixed timing parameters of current pulse)

	Generated SET pulse width model LUT				
	Input 1	Input 2		Input 2 ^p - L	
LET _{DRIVE}	LET _{DRIVE} (1)	LET _{DRIVE} (2)		LET _{DRIVE} (2 ^P – L)	
b ₀	b ₀ (1)	b ₀ (2)		b₀(2 ^p – L)	
b 1	b1(1)	b1(2)		b₁(2 ^P − L)	
b ₂	b ₂ (1)	b ₂ (2)		$b_2(2^p-L)$	
b ₃	b ₃ (1)	b ₃ (2)		b ₃ (2 ^p – L)	
b ₄	b ₄ (1)	b ₄ (2)		b₄(2 ^p − L)	
b ₅	b ₅ (1)	b₅(2)		b₅(2 ^P − L)	
b ₆	b ₆ (1)	b ₆ (2)		b ₆ (2 ^p – L)	
b ₇	b ₇ (1)	b ₇ (2)		b ₇ (2 ^p – L)	
b ₈	b ₈ (1)	b ₈ (2)		b ₈ (2 ^p – L)	
b ₉	b ₉ (1)	b ₉ (2)		b ₉ (2 ^p – L)	

Figure 4.28: A generic 2D LUT for storing the coefficients for generated SET pulse width model, for a particular gate and all input vectors (for one sensitive node in target gate, and fixed timing parameters of current pulse)

Propagated SET pulse width model LUT				
	Input 1	Input 2		Input P
<i>c</i> ₀	c ₀ (1)	c _o (2)		с ₀ (Р)
<i>c</i> ₁	c1(1)	c1(2)		c1(P)
<i>c</i> ₂	c2(1)	c2(2)		c ₂ (P)
<i>c</i> ₃	c3(1)	c₃(2)		с ₃ (Р)
c ₄	c4(1)	c4(2)		c₄(P)
c ₅	c ₅ (1)	c5(2)		с ₅ (Р)
c ₆	c ₆ (1)	c ₆ (2)		с ₆ (Р)

Figure 4.29: A generic 2D LUT for storing the coefficients for propagated SET pulse width model, for a particular gate and all input pins

In Table 4.25, the number of LUTs and total number of elements, for three SET sensitivity models, are given. If we consider a three-input gate with 8 possible input levels, a corresponding LUT with coefficients for critical charge model will have 64 values. On the other hand, for storing the original simulation data, 8×64 LUTs with a total of 8192 values are required. This shows that the proposed optimization approach can reduce the number of elements in the SET database by more than 2 orders of magnitude.

LUT type	No. of LUTs	No. of elements
Critical charge LUT	1	$8 \cdot (2^P - L)$
Generated SET pulse width LUT	1	$11 \cdot (2^{P} - L)$
Propagated SET pulse width LUT	1	8·P

Table 4.25: Number of LUTs and elements in LUTs for storing the model coefficients for one gate type

As elaborated in Section 4.6, the proposed SET sensitivity models are based on certain simplifications and still do not consider all contributing parameters. Considering all possible dependencies with a single fitting relation is not possible due to complex relations between the contributing parameters. Therefore, when the number of parameters is increased, the number of model LUTs will also increase. For example, if characterization is done for four timing constants of the current pulse, in would be necessary to construct four critical charge LUTs and four generated SET pulse width LUTs. Nevertheless, as the increase of the number of parameters increases the number of original LUTs with characterization data, the LUTs obtained with the derived models will always have significantly smaller number of elements.

4.9 Summary

This chapter has introduced an approach for SPICE-based characterization and modeling of SET effects in standard combinational cells. The presented approach features reduced number of simulations during the characterization, enhanced SET sensitivity models, and reduced SET sensitivity database for subsequent SER evaluation.

Specifically, the following are the main achievements:

- A unified methodology for characterization of the SET sensitivity of standard combinational cells and their hardened configurations is proposed.
- Analytical models for SET generation and propagation effects in standard combinational cells are derived by fitting the simulation results and applying the principle of superposition to capture the complex dependences. The proposed models have the relative error below 10 % compared to SPICE simulations for most analyzed cases, which is acceptable accuracy for evaluation of SET sensitivity of standard logic cells.
- It is shown that the number of simulations during characterization process can be reduced by almost 50 %, by exploiting the fact that the SET sensitivity (critical charge and generated SET pulse width) is almost the same for multiple input levels for 3- and 4-input gates.

- An optimized SET database format based on storing the fitting coefficients of derived models in LUTs is proposed. This allows to reduce significantly the amount of characterization data and the number of LUTs compared to standard approach based on storing the raw simulation data.
- The applicability of the proposed critical charge model to two application-specific standard cells (C-element and SEL protection switch) is verified.
- It is shown that the standard delay cells based on skew-sizing are the most sensitive standard cells, with the SET pulses several hundred ps longer than in other cells.
- It is shown that the load may have strong impact on the SET generation in application-specific standard cells such as SEL protection switch.

The performed characterization of standard combinational cells could serve as a basis for establishment of a comprehensive multi-level rad-hard design flow, as depicted in Figure 3.1 (see Section 3.1). Besides the need to integrate the standard cell library characterization into a comprehensive SER evaluation flow, further work will involve:

- **Experimental evaluation**: To validate the simulation results and proposed models with realistic combinational test circuits and radiation exposure.
- Automation of the SET characterization process: This can be achieved with OCEAN scripts which are supported by the Virtuoso toolkit. The automation should provide fully autonomous parametric simulations, and automatized build-up of characterization LUTs.
- **Detailed definition of SET characterization database format**: Definition of a suitable format for the SET sensitivity database that will be compatible with the standard design flow.
- Accuracy improvement: Extending the characterization process and proposed SET models by including additional important effects, particularly those associated with technology scaling and layout.

Chapter 5

Mitigation of SET Effects in Standard Combinational Cells

The widely accepted approach for hardening of combinational circuits is based on the selective application of SET mitigation techniques to a subset of the most sensitive gates. While this approach may be efficient and cost-effective, there is neither an optimal technique nor a methodology for selection of the most suitable combination of multiple techniques for an arbitrary design. In that regard, this chapter aims to: (i) widen the range of possible solutions by introducing an alternative technique based on the insertion of decoupling cells at the gate's output, and (ii) provide a detailed characterization of the proposed technique and the stateof-the-art techniques, in order to assess the benefits and limitations of each technique. The discussion is divided into nine sections. Section 5.1 gives a short review of the key issues of gate-level SET mitigation. The concept of SET mitigation with decoupling cells is presented in Section 5.2. Section 5.3 investigates the impact of decoupling cells on the SET robustness of standard logic cells. In Section 5.4, a comparison of the proposed technique and seven existing techniques in terms of the SET robustness improvement, introduced area/delay/power overhead and overall SET mitigation efficiency is presented. In Section 5.5, the application of multiple techniques to a combinational path is analyzed. Section 5.6 analyzes the SET mitigation in standard delay cells, as the most SET-sensitive cells in the investigated library. In Section 5.7, the benefits and limitations of each technique, based on the conducted analysis, are outlined. Finally, Section 5.8 recapitulates the achieved results and introduces the possible directions for future work.

5.1 Introduction

As elaborated in Section 3.4, a variety of SET mitigation techniques can be applied to standard logic cells without changing their internal structure. Since the SET hardening is applied locally (to the most sensitive gates), these techniques are usually referred to as gate-level mitigation (hardening) techniques. However, the limited contribution of individual techniques to the SER improvement, and the introduced penalties in terms of area, delay and power overhead per gate, are the major drawbacks of the existing gate-level mitigation techniques. In general, the mitigation techniques which provide significant enhancement of the SET robustness incur high area, delay or power overhead, whereas the techniques which efficiently address the SET generation usually have weak impact on the SET propagation.

The standard digital libraries are equipped with few sizes per gate type (for most gates the maximum driving strength is x4). Therefore, the gate upsizing has limited applicability for SET generation mitigation, in addition to its inherent limitation related to weak SET filtering. Unless new hardened cells are added to the library, a possible solution is in duplicating the existing cells, but this does not solve the problem of SET propagation. Alternatively, more and more approaches rely on connecting custom-designed redundant logic to the target gate's output in order to increase the node capacitance, and reduce the SET generation and propagation effects. However, besides the obvious cost in terms of area, delay and power overhead, an important issue with the techniques based on connection of redundant components is that the added logic may be also sensitive to particle strikes, potentially increasing the overall SER. It is essential that the redundant logic has negligible SET sensitivity compared to the benefit in terms of the SET robustness improvement. Furthermore, the added logic should not disrupt the normal operation (logic function) of the circuit. For example, the use of cross-coupled inverters, discussed in Section 3.4, imposes the restriction that only minimum sized inverters should be employed in order not to degrade the useful signal propagating through the logic path.

Considering the limitations of existing techniques, we propose a capacitive SET mitigation approach based on the insertion of decoupling cells at the output of target logic gates. **To the best of our knowledge, the use decoupling cells for hardening the combinational gates in bulk CMOS technology has been proposed for the first time in our work** [MA13]. Subsequently, the applicability of decoupling cells for SET mitigation in standard combinational gates designed in FinFET technology has been confirmed by Zimpeck *et al.* [256]. Zimpeck *et al.* have also shown that the insertion of decoupling cells is beneficial for mitigation of process variability effects [292]. As will be demonstrated in the following, the main benefit of the proposed technique over the two most common techniques (gate upsizing and gate duplication) is better SET filtering. However, the introduced area, delay and power overheads may be larger than the gate upsizing and gate duplication. For that reason, the proposed technique must be viewed in the context of combined application with other complementary techniques.

By combining multiple complementary techniques and applying them selectively to a given circuit, the overall system SER can be minimized while keeping the area, delay and power overheads at an acceptable level. However, the lack of unified approach for selecting the optimal mitigation solution for an arbitrary design makes this process very challenging, particularly because every combinational circuit is unique in terms of the number and type of gates, as well as the number of inputs and outputs. As a consequence, the techniques applied to one circuit may not be optimal for another circuit. To facilitate the selection of appropriate SET mitigation techniques for a particular design, we have conducted a detailed characterization of different gate-level solutions to quantify their impact on the SET robustness and the introduced overhead. In such a way, the characterization database for the hardened standard cells can be formed similarly to the characterization database for the SET sensitivity of standard cells, as discussed in Section 4.8. The choice of target gates for applying the SET mitigation techniques is based on ranking of all gates in a target circuit according to their contribution to the SET generation and SET propagation. In that regard, the characterization database for the gate-level SET mitigation techniques can be used to guide the circuit designers in selecting the most appropriate mitigation strategy. Furthermore, this is essential for reducing the SER evaluation runtime for a target design, as there would be no need to perform exhaustive simulations after applying the selected hardening measures.

5.2 Concept of SET Mitigation with Decoupling Cells

Decoupling cells (Decaps) are commonly used for the on-chip filtering of noise on the power supply and signal lines [293, 294]. The supply noise in an integrated circuit is resulting from the inherent resistive (IR) and inductive (Ldi/dt) voltage drops, as well as from the switching of logic levels. Moreover, in mixed-signal designs with multiple power domains, the coupling of noise from one power domain to another, as well as from analog to digital sub-system, may occur. The voltage glitches caused by these affects may adversely affect the operation of digital logic. Therefore, insertion of decoupling cells between the supply and ground terminals of critical elements provides the low-pass RC filtering of noise glitches.

A basic implementation of a decoupling cell consists of one NMOS transistor, with the gate connected to supply rail, while source and drain are shorted to ground, as illustrated in Figure 5.1 (a). A similar implementation can be realized with PMOS transistor, by connecting the gate to ground and drain/source to supply voltage. Alternative implementation consists of one PMOS and one NMOS transistor connected in the cross-coupled fashion, as depicted in Figure 5.1 (b). The cross-coupled design is more commonly used in practice because of its higher robustness to electrostatic discharge (ESD).

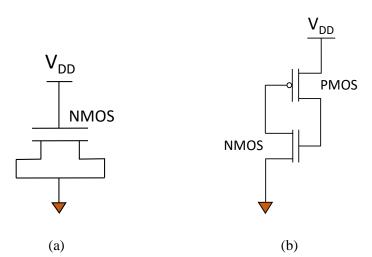


Figure 5.1: Schematic of decoupling cells in CMOS technology; (a) with one NMOS transistor, (b) with cross-coupled NMOS and PMOS transistors

Using the decoupling cells as glitch filters could be effective in SET mitigation. A concept of SET mitigation by insertion of two decoupling cells is illustrated in Figure 5.2, with the example of a NAND gate as a target gate. Instead of connecting the decoupling cells between the supply and ground rails, one cell is connected between the gate's output and supply line, while the other is connected between the gate's output and ground. Insertion of decoupling cells at the gate's output has two effects. First, they act as capacitive hardening elements, resulting in the increase of the total capacitance at the gate's output, and thus in the increase of the critical charge of the output node. In addition, the decoupling cells serve as SET filters, suppressing short SET pulses propagating through the target gate.

The proposed approach with decoupling cells is in functional sense similar to the existing techniques based on insertion of redundant elements, such as cross-coupled inverters [253], charge sharing logic [252], Schmitt trigger [255] and transmission gates [257]. All these techniques increase the node capacitance and

thus assist in SET attenuation. Two decoupling cells are required to ensure that the SET pulses with either positive or negative polarity can be suppressed. Thereby, the SET suppression can be achieved for all possible input levels. If the probability of one polarity of SET pulse is dominant, it would be cost-effective to use only one decoupling cell and thus reduce the area and power overhead. Since the capacitance of decoupling cells is defined by the transistors' size, using the cells with larger PMOS and NMOS transistors is more beneficial in terms of SET mitigation. The capacitance can be also increased by connecting multiple decoupling cells in parallel. However, from the aspect of area saving, the use of larger decoupling cells is more favorable than connecting multiple cells in parallel.

Decoupling cells are available as standard cells in most standard digital libraries. Usually several variants with different sizes (capacitances) exist. The configurations with more than two transistors are also available. In standard implementation, the decoupling cells are by default connected to supply and ground terminals since they are intended to be used for noise filtering on the power supply lines. Therefore, in order to use the decoupling cells for SET mitigation as depicted in Figure 5.2, it is necessary to redesign their layout by replacing the supply and ground pins with the standard input/output pins.

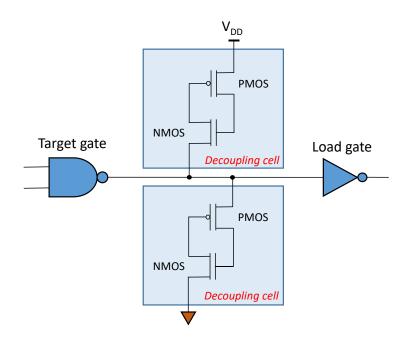


Figure 5.2: Application of two decoupling cells for improving the SET robustness of NAND gate

An important requirement for any gate-level hardening technique is that it does not produce any adverse effects on the normal operation of the target gate. Namely, the use of redundant logic for SET mitigation is effective as long as it does not degrade the useful signal propagating through the target gate. To evaluate the impact of decoupling cells on the normal response of standard logic gates, a series of SPICE simulations have been conducted with different standard cells in IHP's 130 nm digital library and different sizes of decoupling cells. The waveform of the output signal of a NAND2 gate with the driving strength x1, for the cases without decoupling cells and with decoupling cells with drive strengths x1 and x5, are presented in Figure 5.3. The results indicate that the insertion of decoupling cells does not cause degradation of the output signal. Similar behavior was observed for other standard cells in the analyzed 130 nm technology.

This confirms that the proposed approach offers higher flexibility in choosing the transistor sizes than the technique based on the insertion of cross-coupled inverters. Namely, as elaborated in [133], the use of cross-coupled inverters for SET mitigation is restricted to the minimum-sized inverters, as otherwise the useful signal would be degraded.

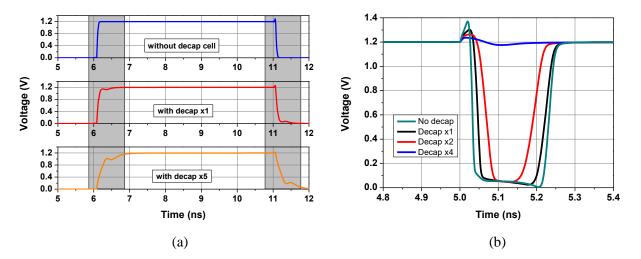


Figure 5.3: Response of NAND2_x1 gate: (a) normal pulse after propagation through NAND2_x1 gate without and with decoupling cells, (b) SET pulses generated at the output of NAND2_x1 gate without and with decoupling cells

Although the decoupling cells do not produce any adverse effect on the normal response of the logic gates, at least for the investigated drive strengths up to x5, due to their capacitive nature the propagation delay will be increased. As the size of decoupling cells is increased, the total capacitance of the output node will increase, and the propagation delay of a target gate will increase accordingly, as can be observed in Figure 5.3 (a). This is due to the charging/discharging of node capacitance, and is reflected in the increase of the low-to-high and high-to-low transition periods. In addition, larger decoupling cells introduce larger area and power overhead, similarly to all existing gate-level hardening techniques.

To estimate the effect of decoupling cell size on the SET sensitivity, the SPICE simulations with the double-exponential current model with fixed rise and fall time constants of 10 and 100 ps, respectively, have been conducted. The results for a NAND2 gate with the minimum driving strength x1 are illustrated in Figure 5.3 (b). For the charge of 80 fC injected in the output node, the amplitude and width of the SET pulse decrease with the increasing size of the decoupling cells, and the SET pulse is completely filtered when the decoupling cells with drive strength x4 are applied. As the critical charge of NAND gate without decoupling cells in the investigated case is around 57 fC, this confirms the capability of the proposed approach to enhance the SET robustness of individual logic gates.

5.3 Analysis of SET Mitigation with Decoupling Cells

After initial evaluation of the impact of decoupling cells presented in previous section, in this section a detailed analysis of the dependence of SET sensitivity of standard logic gates on the driving strength of decoupling cells is conducted. The decoupling cells with drive strengths x1, x2 and x4 have been chosen.

The transistor sizes and respective areas for decoupling cells have been adopted from the standard digital library in IHP's 130 nm technology. Details of the transistor sizes and areas are given in Table 5.1.

Decoupling cell	Transistor size	Cell area (µm ²)
DECAP_x1	$W_{PMOS} = 1.21 \mu m, L_{PMOS} = 450 nm$ $W_{NMOS} = 880 nm, L_{NMOS} = 450 nm$	4.7628
DECAP_x2	$W_{PMOS} = 2.42 \ \mu\text{m}, \ L_{PMOS} = 450 \ \text{nm}$ $W_{NMOS} = 1.76 \ \mu\text{m}, \ L_{NMOS} = 450 \ \text{nm}$	7.938
DECAP_x4	$W_{PMOS} = 4.84 \ \mu m, \ L_{PMOS} = 450 \ nm$ $W_{NMOS} = 3.52 \ \mu m, \ L_{NMOS} = 450 \ nm$	12.7008

Table 5.1: Transistor size and area for decoupling cells in 130 nm technology

To evaluate the effectiveness of decoupling cells for SET mitigation in standard combinational cells, the SPICE simulations with eight most commonly used logic gates (INV, BUF, AND, NAND, NOR, OR, XOR and XNOR) have been performed. The gates with drive strength x1 have been analyzed because these gates are most abundant in digital designs, and also most sensitive to SETs. For each logic gate, with and without decoupling cells, the SET sensitivity has been studied in terms of four metrics: critical charge (Q_{CRIT}), nominal SER, generated SET pulse width and propagated SET pulse width. All simulations have been done for the nominal supply voltage (1.2 V) and temperature of 27 °C.

The characterization methodology used for standard cells in Chapter 4 was employed. The doubleexponential current model was used for critical charge analysis, and the bias-dependent current model for SET pulse width generation analysis. For both models, the fixed timing constants $\tau_{rise} = 10$ ps and $\tau_{fall} = 100$ ps have been chosen. During simulations, the charge was varied in the double-exponential model, while the LET was varied in the bias-dependent model. For the SET propagation analysis, the rectangular voltage pulse with 10 ps rise and fall time constants was injected at the input of target gate, and the output pulse width was observed for different input pulse widths. In all simulations, an inverter with the drive strength x1 was used as a load, and a buffer with the drive strength x1 was used to drive the target gate.

5.3.1 Critical Charge Analysis

For each logic gate investigated in this study, the absolute and normalized critical charge as a function of decoupling cells driving strength was evaluated. The normalized value of critical charge was determined as the quotient of the critical charge value for the case with decoupling cells and the critical charge value obtained for the target gate without decoupling cells. Figure 5.4 illustrates the absolute and normalized critical charge values for 1-input gates (INV and BUF), for the three investigated sizes of decoupling cells and all input levels. In Figure 5.5, the results for six 2-input gates and all input levels are presented. The same analysis was repeated for all gates with 3 and 4 inputs and all input levels. For the sake of brevity, the comparison of the absolute and normalized critical charge of 2-, 3- and 4-input gates is illustrated only for NAND gate, with low input levels, in Figure 5.6.

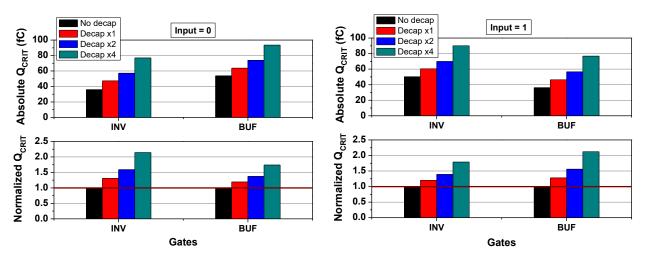


Figure 5.4: Absolute and normalized Q_{CRIT} when two decoupling cells with driving strengths x1, x2 and x4 are inserted successively at the output of 1-input gates (for all input levels)

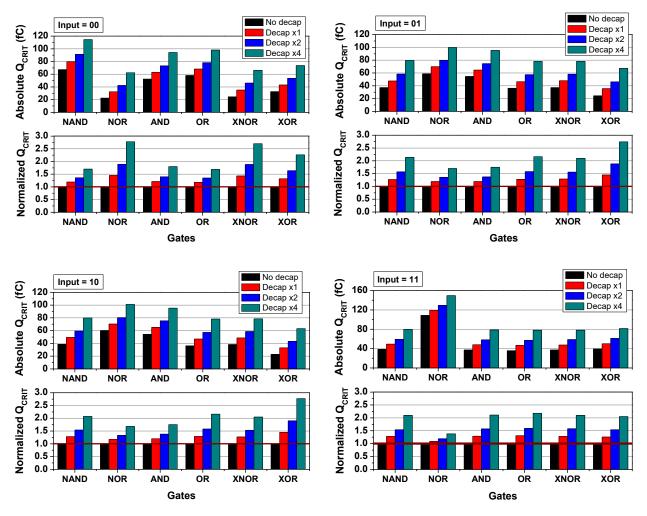


Figure 5.5: Absolute and normalized Q_{CRIT} when two decoupling cells with driving strengths x1, x2 and x4 are inserted successively at the output of 2-input gates (for all input levels)

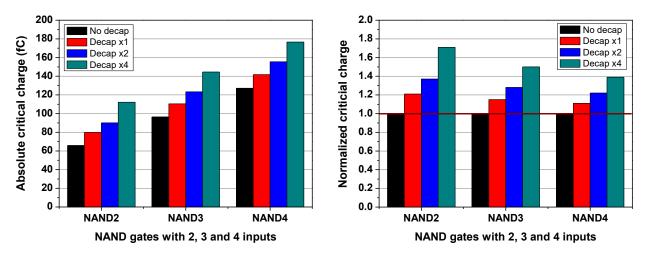


Figure 5.6: Absolute and normalized Q_{CRIT} when two decoupling cells with driving strengths x1, x2 and x4 are inserted successively at the output of 2-, 3- and 4-input NAND gate (for low input levels)

Based on the results depicted in Figures 5.4 - 5.6, the impact of decoupling cells on the critical charge can be summarized as follows:

- The insertion of decoupling cells with a predefined size (driving strength) at the output of a logic gate results in almost the same increase of the absolute value of critical charge, for all investigated gates and all input levels.
- By increasing the size of decoupling cells, the absolute value of the critical charge of a target gate increases linearly, for the investigated decoupling cell sizes from x1 to x4.
- The relative increase of critical charge (with decoupling cells versus without decoupling cells) is larger if the initial value of the critical charge (without decoupling cells) is lower.

The absolute increase of critical charge with DECAP_x1 is from 10 to 13 fC per gate. If DECAP_x2 cells are applied, the critical charge increases roughly by 10 fC more than with DECAP_x1. Similarly, if DECAP_x4 is applied, the critical charge will increase by approximately 20 fC more than with DECAP_x2. Such dependence of critical charge on decoupling cells size can be expected since the linear increase in node capacitance results in linear increase of the corresponding critical charge according to the fundamental critical charge model, $Q_{CRIT} = C \times V_{DD}$.

Therefore, the dependence between critical charge and size of decoupling cells can be conveniently represented in an analytical form using the critical charge modeling approach described in Section 4.6.1. If the critical charge without decoupling cells is denoted as Q_{CRIT} (without decap), then the critical charge after inserting the decoupling cells Q_{CRIT} (with decap) can be expressed as,

$$Q_{CRIT}(with \, decap) = Q_{CRIT}(without \, decap) + S_D \cdot \Delta Q_{CRIT}$$
(5.1)

where S_D denotes the sizing ratio of decoupling cells (1, 2 and 4 in this case) and ΔQ_{CRIT} is the increase of critical charge with DECAP_x1. For the sake of convenience, the value of ΔQ_{CRIT} can be taken as an average value between 10 and 13 fC. This representation allows for fast estimation of the impact of decoupling cells on the SET robustness of individual gates. Since the critical charge of all standard cells without decoupling

cells is obtained during the standard library characterization process, as elaborated in Chapter 4, and the fixed value of ΔQ_{CRIT} can be adopted for all cells, using relation (5.1) eliminates the need to repeat the simulations after insertion of decoupling cells. Nevertheless, it is important to state that the value of ΔQ_{CRIT} will differ if the transistor sizes in the decoupling cells are changed.

Depending on the initial value of the critical charge (without decoupling cells), the relative increase of the critical charge when decoupling cells are applied is from 18 to over 200 %. The largest relative increase is for NOR and XOR which have the lowest critical charge (below 25 fC) for the most sensitive input levels. This implies that the decoupling cells are most effective for hardening the logic gates with lower critical charge. It is be possible to increase further the critical charge by using the decoupling cells with larger capacitance/size.

However, it is important to mention that the insertion of decoupling cells has weaker impact on the critical charge of internal nodes in complex gates composed of multiple simpler gates such as AND and OR. That is because the decoupling cells increase the capacitance only on the output node. Nevertheless, due to the filtering capability of decoupling cells, they can suppress to certain extent the SET pulses generated at the internal nodes of logic gates.

5.3.2 Nominal SER Analysis

Although the insertion of decoupling cells increases the critical charge of the gate's output node, it also increases the total area that can possibly be exposed to particle strikes. Therefore, the possible SET effects resulting from the particle strikes in the decoupling cells, i.e., the contribution of decoupling cells to the overall SER of the target gate, need to be considered. The total nominal SER of a target gate with applied decoupling cells can be determined as,

$$SER_{GATE+DECAP} = SER_{GATE} + SER_{DECAP}$$
(5.2)

where SER_{GATE} denotes the SER of the target gate with the applied decoupling cells for the case when the particle strike occurs in the target gate, and SER_{DECAP} represents the contribution of decoupling cells to the total nominal SER when a particle strikes the decoupling cells. As decoupling cells contribute to both SER components, it is essential to have as low SER_{DECAP} as possible.

To calculate SER_{GATE} and SER_{DECAP} , the empirical SER model defined by relation (2.3) (see Section 2.4.3) was employed. This model gives a nominal SER of a gate (soft error generation probability) in terms of critical charge and sensitive area. In this study, the sensitive area was determined as the drain area of the off-state transistors. The critical charge of the target gate with and without applied decoupling cells was determined in previous section. In a similar way, the critical charge of decoupling cells was determined by injecting the current in the PMOS and NMOS transistors of the decoupling cells and observing the corresponding SET pulse at the output of load gate. Without loss of generality, the SER was analyzed for the most sensitive input levels and with DECAP_x1 cells connected at the output of each gate. Therefore, this analysis considers the worst case nominal SER.

In Table 5.2, the critical charge values for 1- and 2-input gates with decoupling cells are presented. The results indicate four values of critical charge: (i) when the current is injected in the output node of a gate

without decoupling cells, (ii) when the current is injected in the output node of a gate with applied decoupling cells, (iii) when the current is injected in PMOS transistor of decoupling cells connected to the target gate, and (ii) when the current is injected in NMOS transistor of decoupling cells connected to the target gate. By comparing the obtained values, it can be seen that the critical charge due to particle strikes in decoupling cells is for approximately 30 fC higher than for the case when the particle strikes the target gate without decoupling cells. This implies that decoupling cells are inherently more robust to SETs than standard logic cells, which is a critical requirement for added redundant logic to qualify as an efficient SET mitigation technique.

Target gate (most sensitive input level)	Q _{CRIT} for strike in output node without DECAPs (fC)	Q _{CRIT} for strike in output node with DECAP_x1 (fC)	Q _{CRIT} for strike in PMOS transistor in DECAP_x1 (fC)	Q _{CRIT} for strike in NMOS transistor in DECAP_x1 (fC)
INV (0)	35.9	47.2	57.9	62.7
BUF (1)	36.2	46.3	58.4	58.2
NAND2 (11)	38.5	48.9	67.3	71.1
AND2 (11)	37.2	48.1	66.1	66.8
NOR2 (00)	22.4	32.6	51.2	52.5
OR2 (11)	35.8	47.7	66.7	68.3
XOR2 (10)	22.8	33.1	54.5	56.2
XNOR2 (00)	24.5	35.1	53.2	53.9

Table 5.2: Critical charge for standard logic gates without and with applied decoupling cells, when the current pulse is injected successively in the output node of target gate and in decoupling cells connected to the target gate (for the most sensitive input levels)

The calculated SER values for analyzed gates, for the cases with and without decoupling cells, are illustrated in Figure 5.7. The absolute SER values represent the nominal SER for each gate, while the normalized SER values denote the ratio of the SER of a gate with decoupling cells and the SER of a gate without decoupling cells. It can be seen that the insertion of decoupling cells decreases the SER of all analyzed gates, even though the total sensitive area is increased. That is because, according to the SER model defined by relation (2.3) (see Section 2.4.3), the increase in area due to decoupling cells leads a linear increase of gate SER, but simultaneously the increase in Q_{CRIT} results in exponential decrease of SER. Depending on the type of gate, for the analyzed case with the most sensitive input levels, the insertion of decoupling cells reduces the SER by at least 15 % per gate. It should be considered that when the impact of decoupling cells on the SET filtering is taken into account, the overall SER including electrical and timing masking factors would be further reduced. Due to the applied simplifications (not considering the real particle flux), the real SER values would be different from those presented. Nevertheless, as the same simplifications in calculation have been applied to both cases (with and without decoupling cells), the deviation from the real SER values would be similar.

As can be observed in Figure 5.7, the decrease of SER per gate is non-uniform. For example, decoupling cells provide larger SER decrease for inverter than for buffer. Similarly, larger SER decrease occurs for NAND2 than for AND2. This can be explained by the fact that decoupling cells, being external capacitive

elements, primarily affect the sensitivity of the gate's output node. Thus, for complex gates with more transistors, the change of critical charge of internal nodes due to added decoupling cells would be weaker, as mentioned in previous discussion. The SER decrease when decoupling cells are applied to 3- and 4-input gates would be similar in terms of absolute change because the critical charge of decoupling cells is the same regardless of the type of target gate. In order to reduce further the SER, decoupling cells with larger size should be applied.

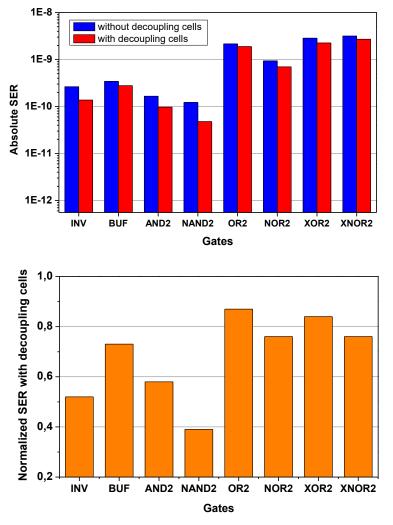


Figure 5.7: Absolute and normalized SER for 1- and 2-input standard logic gates with and without decoupling cells with size factor x1, for the most sensitive input levels

5.3.3 SET Pulse Generation Analysis

For analysis of the SET pulse width generated at the output of a target gate as a function of decoupling cell size, the bias-dependent current pulse was injected at the output of each gate. The LET was varied from 0.5 to 30 MeVcm²mg⁻¹. Based on the acquired results, the two main observations are:

• For LET values up to 3 MeVcm²mg⁻¹, the generated SET pulse width decreases as the decoupling cell size is increased.

• For LET values above 3 MeVcm²mg⁻¹, the generated SET pulse width increases with the increase of the decoupling cell size. This is due to the loading effect of decoupling cells and is similar to the effect of increasing the fan-out.

To illustrate the observed effects, the results for NAND2 gate are depicted in Figure 5.8. The shaded area indicates the "SET pulse width – LET" region where the decoupling cells are effective in reducing the generated SET pulse width. These results indicate that the use of decoupling cells is most effective in mitigation of SETs induced by the low-LET particles. This is consistent with the well-known fact that the gate-level SET mitigation techniques are mostly effective against short SETs induced by the low-LET particles. It is important to recall that the low-LET particles are more abundant than the high-LET particles in space.

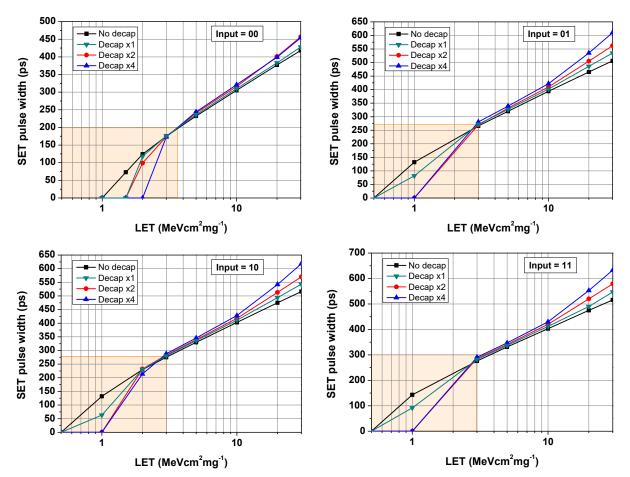


Figure 5.8: SET pulse width at the output of NAND2_x1 gate as a function of LET, when decoupling cells with driving strengths x1, x2 and x4 are applied successively (for all input levels)

In order to compare the impact of decoupling cells on the suppression of short SETs in different logic gates, the generated SET pulse width for the cases with and without decoupling cells is presented in Table 5.1. In all cases the current pulse with LET = $1 \text{ MeV cm}^2\text{mg}^{-1}$ was injected in output node of the target gate. This LET value is above the threshold LET for all investigated gates. The analysis was done for the most sensitive input level (for lowest critical charge). The results indicate that the decoupling cells can suppress

the generated SET pulse width by more than 30 % when the pulse width is below 200 ps. It is important to note that for all logic gates where the generated SET pulse without decoupling cells is less than 200 ps, the use of larger decoupling cells can completely filter the SETs.

Target gate	Gener	ated SET pulse widtl	h (ps)
(most sensitive input)	Without DECAP	With DECAP_x1	SET pulse width decrease (%)
INV (0)	131	89	32
BUF (1)	133	87	35
NAND2 (11)	138	86	38
NAND3 (111)	200	180	10
NAND4 (1111)	245	237	3.3
AND2 (11)	132	81	39
AND3 (111)	130	74	43
AND4 (111)	126	67	47
NOR2 (00)	244	203	17
NOR3 (000)	323	321	0.6
NOR4 (0000)	131	85	35
OR2 (11)	135	88	35
OR3 (111)	130	74	43
OR4 (1111)	126	67	47
XNOR2 (00)	265	259	2
XNOR3 (000)	329	326	1
XOR2 (10)	259	254	1.9
XOR3 (100)	264	263	0.4

Table 5.3: Width of SET pulse generated at the output of logic gates with driving strength x1, when the current pulse with $LET = 1 \text{ MeVcm}^2\text{mg}^{-1}$ is injected in the output of each gate (for most sensitive input levels)

5.3.4 SET Pulse Propagation Analysis

The capability to filter (mask electrically) the propagating SET pulse is an essential parameter for evaluating the effectiveness of a SET mitigation technique. Considering that the propagation delay of standard logic gates defines the SET filtering capability (gates with larger delay are more likely to filter SET pulses), the objective of the gate-level hardening is to enhance the SET filtering by increasing the propagation delay of individual gates in the circuit. To study the SET filtering capability of the proposed technique, the relation between the input pulse width and the output pulse width for the cases with and without decoupling cells was studied. The input pulse width was varied from 50 to 200 ps since this is the typical range of SET pulse widths that can be suppressed by the gate-level mitigation techniques. Without loss of generality, we have considered only the input pulses with the positive polarity and amplitude equal to supply voltage. It is important to note that the simulation setup was composed of a driver buffer with drive strength x1 connected

to the input of target gate, and a load inverter with drive strength x1. The delay was observed from the input of diving buffer to the output of load inverter. Thus, for different drive and load gates the results may differ, but the general trend would be similar.

In Figure 5.9, the impact of decoupling cells on the SET filtering capability of NAND2 and NOR2 gates is illustrated. It can be noticed that the insertion of decoupling cells has different impact on the two gates. The SET suppression is stronger for NAND2 gate, while for NOR2 gate it is necessary to apply DECAP_x4 to achieve substantial SET suppression. This difference comes from the difference in the node capacitances of the two gates and their propagation delays. Similar trend was observed for other analyzed gates. In general, two important effects of decoupling cells on the SET pulse propagation through a logic gate have been observed:

- The decoupling cells with drive strength up to x4 can attenuate or completely filter the input SET pulses shorter than 300 ps. The filtering effect depends on the type of target gate, and is stronger for shorter input SETs. Using larger decoupling cells provides better SET filtering and enables to completely filter the short SETs (less than 100 ps).
- By increasing the size of decoupling cells, the minimum SET pulse width that can propagate through a target gate increases. This effect is due to the increase of the propagation delay with the increase of the size of decoupling cells.

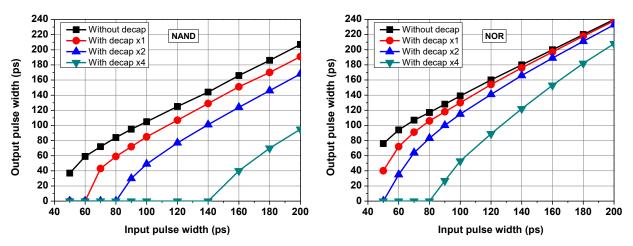


Figure 5.9: Effect of decoupling cells on SET filtering for NAND2 and NOR2 gates

In order to quantify the SET filtering capability of decoupling cells, the minimum SET pulse width that can propagate through a target gate was analyzed for different driving strengths of decoupling cells applied to the gate's output. The results are presented in Table 5.4. With the increasing size of decoupling cells, the minimum input pulse width that can propagate through a gate increases linearly. This confirms that larger decoupling cells are more effective in SET suppression. This is consistent with previous discussion which has shown that larger decoupling cells increase the robustness to direct particle strikes. It is necessary to mention that different values from those given in Table 5.4 may be obtained if other types and sizes of driving and load gates are used. Nevertheless, the relative change of the SET pulse width would be similar as in the analyzed case. It is interesting to note that the filtering effect of decoupling cells is more pro-

nounced for more complex gates. For example, the absolute increase of the minimum SET pulse width is largest for XOR and XNOR gates.

Target gate	Minimum width of input pulse that can propagate through the target gate (ps)				
	No DECAP	DECAP_x1	DECAP_x2	DECAP_x4	
INV	30	42	60	94	
BUF	45	65	85	155	
NAND2	50	70	90	160	
NAND3	60	90	140	220	
NAND4	75	125	180	290	
AND2	70	90	120	160	
AND3	95	120	145	195	
AND4	120	140	165	220	
NOR2	40	50	60	90	
NOR3	46	60	75	100	
NOR4	55	62	70	80	
OR2	52	60	90	140	
OR3	50	65	80	120	
OR4	60	75	95	145	
XNOR2	60	80	110	190	
XNOR3	55	85	125	200	
XOR2	60	75	155	280	
XOR3	70	100	170	320	

Table 5.4: Minimum pulse width that can propagate through a logic gate with drive strength x1, without and with decoupling cells

5.3.5 Application of Decoupling Cells to Combinational Paths

To evaluate the impact of decoupling cells on the SET propagation in a realistic combinational circuit, two logic paths have been investigated:

- (i) A homogeneous NAND path composed of ten NAND2 gates with driving strength x1.
- (ii) A heterogeneous NAND-NOR path composed of five NAND and five NOR gates with driving strengths x1 and x2.

Choice of combinational paths as target circuits is relevant since the gate-level hardening techniques are applied to the sensitive gates in individual logic paths which constitute a complex circuit, and the SET sensitivity of any complex circuit is assessed by analyzing the SET effects in each path. The path length of ten gates was chosen because most logic paths between flip-flops in modern circuits have less than ten gates. As has been demonstrated in Section 4.4.4, short logic paths may be particularly vulnerable to the propagation-induced SET pulse broadening. The NAND and NOR gates have been chosen because they

are, together with inverters, the most common logic gates in digital designs. The analyzed logic paths, with the applied decoupling cells, are illustrated in Figure 5.10 and Figure 5.11.

The first gate in the path was selected as a target node and the bias-dependent current source with fixed rise and fall time constants (10 and 100 ps) was used to inject the current in the output of the target node. As previous analysis has shown that DECAP_x4 is most effective for SET mitigation, it was used for this analysis. To analyze the impact of decoupling cell position on the SET sensitivity, one and two pairs of decoupling cell have been inserted at different nodes along the path. The choice of the position for inserting decoupling cells is somewhat arbitrary, as in a combinational path without logical masking any gate may be sensitive. To eliminate logical masking, the controlling inputs of all gates were set to logic levels which allow the signal propagation. The dependence of the SET pulse width at the output of the path as a function of LET, for different positions of decoupling cells, is illustrated in Figure 5.10 (for NAND path) and in Figure 5.11 (for NAND-NOR path).

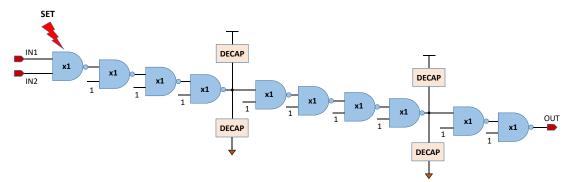


Figure 5.10: Homogeneous path with NAND gates and decoupling cells at nodes 4 and 8

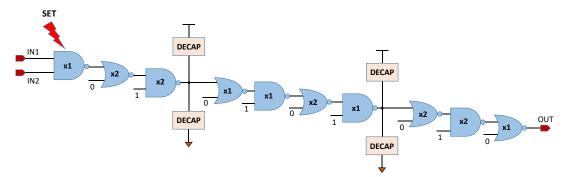


Figure 5.11: Heterogeneous path with NAND and NOR gates and decoupling cells at nodes 3 and 7

As can be observed in Figure 5.12 and Figure 5.13, the position (circuit node) where the decoupling cells are inserted has strong impact on the SET suppression. For NAND path, insertion of decoupling cells at nodes 4 or 8 results in a decrease of output SET pulse width by around 150 ps for the investigated LET range from 0.5 to 30 MeVcm²mg⁻¹. However, inserting the decoupling cells at node 1 is not recommendable as the SET pulse width will increase for high LET values due to the previously described loading effect. By inserting the decoupling cells at two nodes (1/4, 1/8 or 4/8), the SET pulse width can be also reduced. The best results can be achieved by inserting the decoupling cells at nodes 4/8, thus reducing the output SET pulse width by almost 200 ps. It is important to note than inserting the decoupling cells at nodes 4 or

8 is more effective in SET suppression than inserting the decoupling cells at nodes 1/4 or 1/8. However, the situation is significantly different in the case of NAND-NOR path, where inserting even two decoupling cells at certain nodes may be ineffective. For example, in the NAND-NOR path the best SET suppression is achieved by placing decoupling cells at nodes 3 and 7, while placing the cells at nodes 4 and 8 results in longer SETs than without decoupling cells.

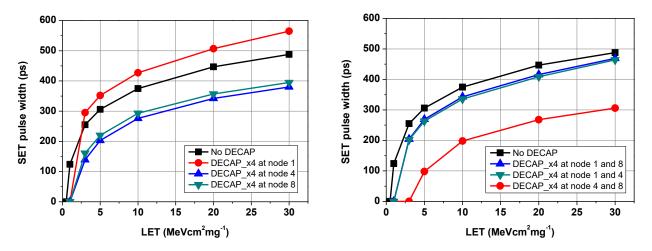


Figure 5.12: SET pulse width at the output of a 10-gate NAND path as a function of LET, for different positions of decoupling cells with size factor x4

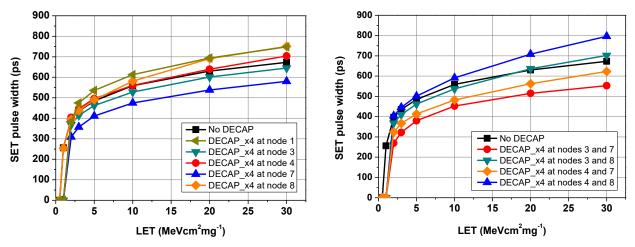


Figure 5.13: SET pulse width at the output of a 10-gate NAND-NOR path as a function of LET, for different positions of decoupling cells with size factor x4

The reason for significant difference in SET response between the two analyzed logic paths comes from the difference in the type and size of the constitutive gates. As the NAND path is composed of the same gates with the same driving strength, the broadening of SET pulse during propagation is less than 100 ps. On the other side, in the NAND-NOR path the SET pulse is broadened by approximately 170 ps while propagating through the path. Due to different drive strengths, the pulse broadening varies across the NAND-NOR path. The pulse broadening at nodes 3 and 7 is larger than at nodes 4 and 8. Moreover, nodes 4 and 8 are both NOR gates, while nodes 3 and 7 are NAND gates. As can be seen from data in Table 5.4, decoupling cells are more effective in filtering the SET pulses passing through NAND gate than through

NOR gate. This explains why inserting decoupling cells at nodes 4 and 8 of NAND-NOR path has negative effect (SET is further broadened), while inserting the decoupling cells at nodes 3 and 7 produces the best SET suppression. It can be concluded, based on the acquired simulation results, that from the aspect of SET filtering it is more beneficial to insert the decoupling cells at multiple nodes in the sensitive path, and the target nodes for inserting the decoupling cells should be chosen by considering both the pulse broadening through the gates and the impact of decoupling cells on the respective gates.

5.4 Comparative Analysis of SET Mitigation Techniques

In order to evaluate the qualitative and quantitative impacts of gate-level SET mitigation techniques in standard combinational gates, a comparative characterization of the proposed approach based on insertion of decoupling cells and seven existing techniques has been conducted. The SET mitigation techniques considered in this study are given in Table 5.5. For each technique a short notation to be used in the following discussion is introduced. A more detailed description of the first seven techniques listed in Table 5.5 can be found in Section 3.4. The standard logic gates from IHP's 130 nm digital cell library have been used as target gates.

Technique	Short notation	Short description
Gate upsizing	GU	A target gate is replaced by the same type of gate with higher driving strength
Gate duplication	GD	A target gate is duplicated by connecting its inputs and outputs to an identical copy
Guarded dual modular redundancy	GDMR	A target gate is duplicated and connected to a guard gate and an inverter
Load upsizing	LU	A load gate connected to a target gate is replaced by the same gate with higher driving strength
Insertion of charge sharing logic	CSL	Two inverters are connected to the output of a target gate while their outputs are shorted and floating
Insertion of transmission gates	TG	Two transmission gates are connected to the output of a target gate
Insertion of Schmitt trigger	ST	A Schmitt trigger with an inverter is connected to the output of a target gate
Insertion of decoupling cells	DECAP	Two decoupling cells are connected to the output of a target gate

Table 5.5: Gate-level hardening configurations analyzed in this work

The obtained results can serve as a basis for constructing a characterization database for the gate-level SET mitigation techniques. Such a database would enable to rank the analyzed techniques in terms of their quantitative and qualitative contribution to the SET robustness improvement for each logic gate, and the

introduced area, delay and power overhead. This information may be used as a guideline for the designers in choosing the most efficient and cost-effective SET mitigation strategy for a given circuit. In particular, the ranking of the SET mitigation techniques in terms of their quantitative impact on SET robustness is useful for combined application of multiple techniques, allowing to exploit their complementary advantages and therefore minimize the impact of their individual weaknesses.

For the sake of fair comparison, the same transistor sizes have been selected for all techniques and the target gates with the minimum drive strength x1 have been used. Without loss of generality, the analysis was done for gates with 1 and 2 inputs. Similar trends have been observed for the corresponding 3- and 4-input gates. It is important to mention that here we have not considered the standard SET filtering technique based on delay and a guard gate [259, 260] because of the high delay overhead incurred by this approach. Similarly, we have not analyzed the SET filtering based on insertion of cascaded inverters [146] due to the necessity to use one large inverter, which leads to excessive area overhead per gate. Nevertheless, both of these techniques may be considered in cases when the delay and area overhead are not critical. The idea of the presented comparison is to evaluate the techniques which incur as low overheads as possible, and assess their applicability as alternatives to the SET filtering techniques based either on delay element and guard gate, or cascaded inverters.

5.4.1 Comparison of SET Sensitivity

The comparative evaluation of the gate-level SET mitigation techniques has been done with SPICE simulations, using the same setup as in previous discussion. For each gate and each hardening configuration listed in Table 5.5, the SET sensitivity was assessed in terms of the standard SET generation and SET propagation metrics. Thus, the effectiveness of each technique on both the SET generation and SET propagation can be assessed individually.

5.4.1.1 Critical Charge Comparison

In Table 5.6, the critical charge values for 1- and 2-input standard logic gates, without applied hardening and with each hardening configuration, are given. All critical charge values are determined for the most sensitive input levels for the corresponding logic gate. To illustrate the relative impact of each technique, the normalized critical charge values for NAND2 gate are shown in Figure 5.14.

The highest SET immunity of a target gate to direct particle strikes can be achieved with GDMR. By duplicating the target gate and connecting the outputs of the two copies to a guard gate, the target gate becomes completely robust to SETs, provided that the energetic particle does not hit simultaneously the sensitive transistors in both gates. For this reason, the critical charge is not relevant for the target gates with GDMR configuration, and thus no results for this technique are shown in Table 5.6. However, the transistors in the guard gate and added inverters are sensitive to particle strikes.

Apart from GMDR, the highest increase in critical charge can be achieved with the GU and GD techniques. As seen in Table 5.6 and Figure 5.14, GU can provide over 70 % increase of critical charge when a gate with driving strength x1 is replaced by a gate with driving strength x2. Depending on the type of gate and the input logic levels, the critical charge increase can be lower, but in all cases the GU technique is superior over other techniques in terms of critical charge increase. As the GU is a replacement of a smaller

gate with a larger one from the same library, the results for GU can be obtained directly from the standard cell characterization described in Chapter 4. Almost the same effect can be obtained with gate duplication (GD). However, the major benefit offered by GD is that it can be applied to standard logic cells which cannot be upsized if there are no available higher sizes in the library.

The LU has the weakest impact on critical charge among the analyzed techniques. By increasing the size factor of load inverter from x1 to x2, the critical charge increases by a maximum of 10 %. Though, it is important to mention that we consider here only an inverter as a load gate connected to the output of a target gate. The increase in critical charge would be slightly higher when the load is composed of more complex gates (e.g., AND, OR), but in general the LU remains inferior to other techniques regarding the impact on critical charge.

Among the four techniques based on insertion of external redundant logic (CSL, TG, ST and DECAP), ST provides the highest increase in critical charge while TG provides the lowest increase in critical charge for the size factor x1. All four techniques can increase the critical charge from 10 to 30 % with the size factor of x1. Although the differences between the techniques are relatively small, it is important to note that small increase of critical charge results in significant reduction of SER due to inverse exponential dependence between these two metrics.

Cell	Critical charge (fC)								
configuration	INV	BUF	NAND2	AND2	NOR2	OR2	XNOR2	XOR2	
Standard x1 cell	35.9	36.2	38.5	37.2	22.4	35.8	24.5	22.8	
GU	67.4	67.7	65.5	72.1	43.6	69.2	41.5	47.5	
GD	66.6	67.2	67.7	70.2	41.0	69.5	41.2	46.8	
GDMR	-	-	-	-	-	-	-	-	
LU	40.2	41.2	41.7	41.6	25.4	38.8	28.3	25.9	
CSL	45.2	45.5	46.9	46.3	31.3	45.1	33.2	31.3	
TG	46.1	44.4	46.3	45.4	30.3	46.2	32.2	30.8	
ST	51.7	47.2	50.3	53.9	33.7	48.1	36.2	34.4	
DECAP	47.2	46.3	48.9	48.1	32.4	47.7	35.1	33.1	

Table 5.6: Critical charge at the output node of a target gate (for the most sensitive input levels)

Since all techniques can be applied with different size configurations, it is important to consider the dependence of critical charge on the size factor. Because the GU and GD will have dominant impact on critical charge regardless of the size factor, while the effect of GDRM is independent of its size factor, we have done the comparison for LU, TG, ST, CSL and DECAP. The analysis was conducted for size factors from x1 to x4, and the dependence of critical charge on the sizing factor for NAND2 gate with 11 input is presented in Figure 5.15. Similar results have been obtained for other logic gates. For all techniques, the critical charge increases almost linearly with the size factor. However, as can be observed, this increase differs among the analyzed techniques. The techniques LU, TG, ST and CSL exhibit similar rate of increase of critical charge, i.e., have similar slope of the "critical charge *vs* size factor" dependence. Thus, the analytical model defined by relation (5.1) can be applied to all techniques to estimate the critical charge for a given hardening configuration. The highest increase of critical charge for size factors from x1 to x4 is achieved with DECAP. Although the critical charge with ST is higher than with DECAP for size factor x1,

this is reversed for size factors greater than x2. Thus, it can be concluded that if the use of higher size factors does not violate the design constraints and has no adverse affects on the SET propagation, the DECAP technique would be a better choice for increasing the critical charge than the LU, TG, ST and CSL.

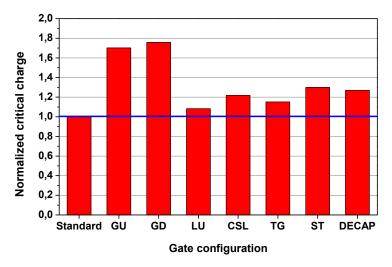


Figure 5.14: Normalized critical charge for standard (non-hardened) NAND2_x1 gate and NAND2_x1 gate with hardening configurations (for 11 input)

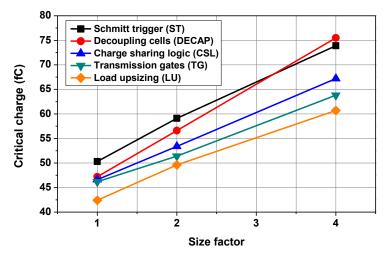


Figure 5.15: Dependence of critical charge on size factor of applied hardening configuration (for NAND2_x1 gate with 11 input)

For estimating the impact of each technique on the overall SER of a logic gate, it is necessary to consider the sensitivity of the added (redundant) logic. This applies to all techniques except GU, GD and LU where the number of sensitive nodes is not changed. As has been shown in previous discussion, the decoupling cells are highly robust to direct particle hits, with the average critical charge being at least for 30 fC higher than for the strikes in the target gate. The most sensitive to particle strikes are GDMR and ST. Although GDMR provides full robustness of the target gate, the added guard gate and the extra inverter are sensitive to particle strikes. Similarly, the added inverter in ST is also sensitive to particle strikes. Among the five techniques (GDMR, ST, TG, CSL and DECAP), only CSL is completely immune to particle strikes in the added logic because this logic is floating (see Figure 3.10 (a)), and therefore a particle strike will not result in an observable SET.

5.4.1.2 SET Pulse Generation Comparison

Along with the effect on critical charge, it is important to evaluate the capacity of mitigation techniques to suppress the generated SET pulse, i.e., to decrease the SET pulse width at the output of a target gate. The higher suppression of the initial SET pulse will increase the probability that it will be electrically masked while propagating through the subsequent logic gates.

In order to investigate the impact of hardening configurations on the generated SET pulse width, a biasdependent current model was used to inject the current pulse with LET = 1 MeVcm²mg⁻¹ at the output of each gate, and the corresponding SET pulse width was observed at the output of respective load inverter. All hardening configurations have been applied with the size factor x1, and the obtained results are presented in Table 5.7. It can be noticed that GU and GD techniques provide the strongest suppression of the generated SET pulse width. For all gates except XNOR2 and XOR2, the initial SET pulses shorter than 250 ps can be completely suppressed by GU or GD. This is in accordance with the fact that these two techniques provide the highest increase in critical charge, as demonstrated in previous section. Similarly to the critical charge analysis, the SET pulse will not be generated in the target gate when GDMR is applied. It can be seen that for other techniques the impact on initial SET pulse width, and in some cases even the SET pulse broadening, occurs for NOR2, XOR2 and XNOR2 gates, for which the initial SET is longer than 250 ps at LET = 1 MeVcm²mg⁻¹.

hardening configurations with size factor x_1 , for $LE_1 = 1$ MeV change										
Cell		SET pulse width generated at output of target gate (ps)								
configuration	INV	BUF	NAND2	AND2	NOR2	OR2	XNOR2	XOR2		
Standard x1 gate	131	133	138	133	244	135	269	265		
GU	0	0	0	0	0	0	100	110		
GD	0	0	0	0	0	0	104	113		
GDMR	-	-	-	-	-	-	-	-		
LU	134	128	148	132	261	132	290	286		
CSL	117	121	108	110	285	110	314	310		
TG	108	111	96	110	291	96	310	276		
ST	0	45	122	0	254	0	287	269		
DECAP	89	92	92	81	242	81	264	259		

Table 5.7: Generated SET pulse width for standard logic gates without hardening and with hardening configurations with size factor x1, for LET = $1 \text{ MeV cm}^2\text{mg}^{-1}$

As discussed previously, due to the loading effect of the added redundant logic, the generated SET pulse width may increase at higher LET values. This effect is not desired and should be taken into account when choosing the appropriate techniques for a particular design. As an example, the generated SET pulse width at the output of NAND2 gate with drive strength x1, for analyzed hardening configurations and LET = 5 MeVcm²mg⁻¹, is presented in Figure 5.16. It can be noticed that loading effect has no relevance for GU and GD techniques, i.e. there is not broadening of generated SET pulse. This is expected since GU and GD do

not add external redundant elements. However, all techniques based on insertion of external elements suffer from the increase of generated SET pulse for higher LET values. This can be observed for several techniques already at LET = 1 MeVcm²mg⁻¹ (see Table 5.7). For the case illustrated in Figure 5.16, the SET pulse width does not increase with DECAP and GMDR techniques, but this effect can also be observed when these techniques are used with higher size factors, as well as for other gates. Among the investigated techniques, the ST results in the highest increase of generated SET pulse width. These results indicate that the GU and GD are the best options when it is required to improve the robustness of a logic gate to direct particle strikes. GDMR may be acceptable if the sensitivity of added logic does not affect the overall SER, which depends on the target circuit design.

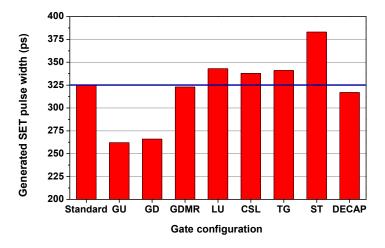


Figure 5.16: Generated SET pulse width at the output NAND2_x1 gate without and with hardening configurations with size factor x1, for LET = $5 \text{ MeV cm}^2 \text{mg}^{-1}$

5.4.1.3 SET Pulse Propagation Comparison

To evaluate the capability of investigated techniques to filter the SET pulses propagating through a single logic gate, the relation between the input and output SET pulse widths was analyzed. A positive rectangular pulse with predefined duration was fed to the input of a target gate to emulate the incoming SET pulse, and the pulse width was observed at the output of load inverter. In Table 5.8, the output pulse widths for standard logic gates without and with hardening configurations, for the input pulse width of 100 ps, are presented. The size factor x1 was used for all hardening configurations. In all cases the positive (0-to-1) input pulse was applied. As can be observed, all analyzed gates cause the pulse broadening even without any hardening techniques, which is most pronounced for NOR and OR gates. It is worth to mention that for negative (1-to-0) input pulse some gates would cause the pulse shrinking. Obviously, the propagation-induced pulse broadening is more critical from the aspect of SET mitigation, and it is thus necessary to consider how individual mitigation techniques address this effect. The broadening or shrinking of the propagating SET pulse is also determined by the type and size of drive and load gates, which are fixed in this case to ease the comparative analysis.

Based on the results in Table 5.8 it can be seen that the impact of GU and GD on SET propagation is significantly weaker compared to their impact on SET generation. The SET filtering can be improved with GU by using gates with higher drive strength. For example, by using the buffers and inverters with drive

strength x12 or more, the short SET pulses (up to 100 ps) can be completely filtered. However, such large sizes are usually not available for other standard logic gates. This implies that GD and GU would have very limited impact on the propagation of longer SETs. On the other hand, the filtering capacity of LU, ST, TG, CSL, DECAP and GDMR techniques largely depends on the type of target gate. For example, ST provides the best SET filtering for 100 ps pulse at the inputs of INV, NAND2 and XOR2 gates, but is not effective for other gates. Similar trend can be noticed for other techniques, with the exception of LU which has similar impact on SET filtering in all cases.

Cell	SET pulse width at gate output (ps)								
configuration	INV	BUF	NAND2	AND2	NOR2	OR2	XNOR2	XOR2	
Standard x1 cell	121	126	113	106	137	171	104	120	
GU	113	121	105	105	146	167	87	120	
GD	112	125	105	106	130	160	74	111	
GDMR	80	139	67	115	112	185	0	50	
LU	126	122	110	100	158	170	100	140	
CSL	136	126	100	82	185	153	81	124	
TG	134	104	109	77	150	154	76	123	
ST	76	131	31	123	109	181	107	0	
DECAP	115	107	93	80	132	149	78	100	

Table 5.8: Propagated SET pulse width for standard logic gates without hardening and with hardening configurations with size factor x1, for positive input pulse of 100 ps

The results in Table 5.8 indicate that the overall SET filtering capability of the hardening techniques with size factor x1 is very low even for the short SET pulses up to 100 ps. This implies that in real circuits would be imperative to employ the hardening techniques with higher size factors. In order to assess the filtering capacity dependence on the size factor of applied hardening techniques, the analysis was repeated for size factors up to x4 and with the input pulse width from 50 to 300 ps. The output SET pulse width as a function of input SET pulse width, for CSL, TG, ST, LU, GDMR and DECAP with the size factor x4, for NAND2 and NOR2 gates, is illustrated in Figure 5.17 and Figure 5.18, respectively. For the sake of clarity, each figure is divided in two figures.

It can be observed that for NAND gate, the CSL, TG, ST, GDMR and DECAP techniques can filter the SET pulses up to 100 ps. The simulation results have shown that these techniques can filter completely the SET pulses shorter than 200 ps with size factor x8 or higher. In the case of LU, the SET pulses up to 50 ps can be filtered completely, while for filtering longer SET pulses it is necessary to apply the size factor x16 or greater. Similar results have been obtained for INV, BUF, AND, XNOR and XOR gates. For NOR gate neither of the analyzed techniques can suppress the SET pulse when the size factor x4 is used. It can be seen that all techniques lead to opposite effect for NOR gate, causing the pulse broadening. Similar pulse broadening effect was observed for OR gate.

According to the obtained results, it is not possible to identify a single technique which could be efficient in SET filtering for every gate, but is rather required to consider individually the impact of each technique on a particular gate. The selection of a suitable technique should consider the pulse broadening features of both the target gates and the applied hardening techniques. In that regard, it is advisable not to apply the hardening techniques directly to gates which exhibit strong broadening effect, but to some of the following gates which cause weaker pulse broadening.

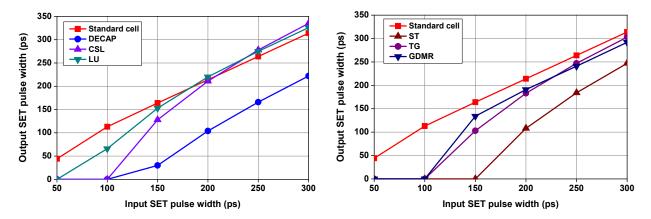


Figure 5.17: Output SET pulse width as a function of input SET pulse width, for NAND2_x1 gate and hardening configurations with size factor x4

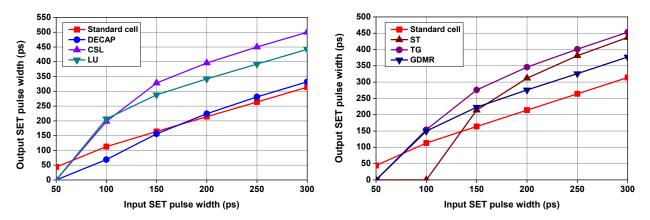


Figure 5.18: Output SET pulse width as a function of input SET pulse width, for NOR2_x1 gate and hardening configurations with size factor x4

5.4.2 Comparison of Area, Delay and Power Overhead

The area, delay and power overhead resulting from the application of SET hardening techniques may be decisive in selection of appropriate technique for a given design. Although each technique may improve the SET robustness, either by reducing the SET generation or the SET propagation effects, the application of a particular technique is justifiable as long as it does not violate the predefined area, delay and power constraints. Excessive area or power overhead may increase the design and exploitation costs, while the delay overhead affects the processing speed of the system and thus the overall performance. In cases when the hardening measures are applied to critical paths in the design, the violation of delay constraints is not acceptable. Since the gate-level SET mitigation techniques are applied selectively to the most sensitive gates in a given circuit, the area/delay/power overhead incurred by the applied mitigation techniques depends on the complexity of target circuit (number of gates in the circuit) and the number of nodes to which the migration techniques are applied. Nevertheless, for the sake of comparison, it is essential to assess the overhead that each technique introduces at the level of individual gates. For this purpose, all hardening

configurations have been analyzed for the size factor x1. Although previous discussion has shown that larger size factors of SET hardening configurations are required to achieve better SET suppression, using the size factor of x1 for overhead analysis gives representative results because the overheads in the case of larger size factors would be proportional to those for size factor of x1.

5.4.2.1 Area Overhead Comparison

Addition of hardware redundancy to mitigate the SET generation and propagation always comes at the cost of increased area. In Table 5.9, the normalized values of area for the standard cells with x1 driving strength and the analyzed hardening configurations are given. All values are normalized by dividing with the area of the respective standard cell with x1 driving strength. As can be seen, the largest area overhead of more than 200 % is introduced by the GDMR and ST techniques, which have the largest transistor count. On the other side, LU has the lowest area overhead of less than 20 %. The DECAP technique has very similar area overhead as the CSL and TG techniques since the number of transistors is the same for these three techniques. It can be noticed that for all techniques based on addition of redundant logic (CSL, TG, ST, and DECAP), the area overhead decreases as the complexity of target gate increases.

Cell	Normalized area									
configuration	INV	BUF	NAND2	AND2	NOR2	OR2	XNOR2	XOR2		
Standard x1 cell	1	1	1	1	1	1	1	1		
GU	1.15	1.15	1.28	1.28	1.13	1.13	1.27	1.27		
GD	1.47	1.58	1.57	1.63	1.57	1.63	1.73	1.73		
GDMR	2.94	2.95	2.92	2.97	2.92	2.97	2.99	2.99		
LU	1.15	1.15	1.14	1.13	1.14	1.13	1.09	1.09		
CSL	1.99	1.86	1.86	1.76	1.86	1.76	1.55	1.55		
TG	1.99	1.86	1.86	1.76	1.86	1.76	1.55	1.55		
ST	2.5	2.3	2.3	2.1	2.3	2.1	1.8	1.8		
DECAP	1.99	1.86	1.86	1.76	1.86	1.76	1.55	1.55		

 Table 5.9: Normalized area for standard logic gates without and with hardening configurations with size factor x1

5.4.2.2 Delay Overhead Comparison

In Table 5.10, the propagation delay for investigated standard logic cells, with and without applied SET mitigation techniques, are given. For easier comparison, the delay was determined from SPICE simulations as the time interval between the rising edge of input pulse and the rising edge of the output pulse in a test circuit composed of a driving buffer, a target gate and a load gate. The input pulse was a rectangular pulse with 5 ns duration. As can be seen, in most cases the smallest delay overhead is introduced by gate upsizing (GU), followed by gate duplication (GD) and load upsizing (LU). This can be explained by the fact that larger gates are faster than smaller ones, for the same load. Thus, the propagation delay of a gate decreases when its size is increased. For the cases presented in Table 5.10 it appears that the delay slightly increases after upsizing because the delay was determined for the path and not for individual gate. On the other hand, the largest delay is introduced by GDMR and ST, which are based on two elements connected in series, and thus have the largest transistor count. Among the techniques with the same number of additional transistors (DECAP, CSL and TG), CSL introduces the smallest delay overhead.

Cell	Delay (ps)									
configuration	INV	BUF	NAND2	AND2	NOR2	OR2	XNOR2	XOR2		
Standard x1 cell	73	103	85	128	75	106	109	145		
GU	74	99	89	119	80	103	110	153		
GD	77	104	89	130	79	109	112	148		
GDMR	173	181	189	203	176	184	220	244		
LU	78	112	96	134	81	110	114	142		
CSL	88	133	109	155	90	136	133	196		
TG	105	149	128	173	109	152	151	210		
ST	156	165	180	189	159	168	206	232		
DECAP	84	123	143	174	104	151	171	252		

 Table 5.10: Propagation delay of a path composed of driving buffer, target gate and load inverter, without and with hardening configurations with size factor x1

5.4.2.3 Power Overhead Comparison

To estimate the power overhead incurred by each hardening configuration, the average power was calculated for a single logic level transition. The power was obtained by simulating the logic transition (change from one logic level to another) and integrating the resulting supply current pulse. This approach is useful for comparative analysis of the dynamic power consumption per gate, but it should be noted that the real power overhead due to hardening measures applied to a particular circuit would depend on the number of target nodes to which the hardening techniques are applied, as well as on the number of gates in the circuit. For the sake of easier comparison, the obtained dynamic power consumption for each configuration was normalized to the corresponding values for standard gates without applied hardening. The results are presented in Table 5.11.

Cell		Normalized power								
configuration	INV	BUF	NAND2	AND2	NOR2	OR2	XNOR2	XOR2		
Standard x1 cell	1	1	1	1	1	1	1	1		
GU	1.02	1.06	1.13	1.21	1.18	1.22	1.25	1.26		
GD	1.06	1.10	1.15	1.23	1.21	1.23	1.27	1.29		
GDMR	2.82	2.89	2.94	2.95	2.94	2.95	2.94	2.94		
LU	1.12	1.13	1.15	1.19	1.17	1.19	1.20	1.20		
CSL	1.86	1.87	1.89	2.02	2.01	2.02	2.05	2.05		
TG	1.92	1.94	1.97	1.99	1.98	2.01	2.03	2.03		
ST	2.65	2.68	2.72	2.75	2.72	2.73	2.73	2.72		
DECAP	1.89	1.92	1.95	1.96	1.95	1.96	1.96	1.94		

 Table 5.11: Normalized power overhead for standard logic gates without hardening and with applied hardening configurations with size factor x1

The SET mitigation techniques which add more transistors result in higher power overhead. Thus, the power overhead trends correspond to the area overhead trends. The highest power overhead per gate is induced by GDMR and ST techniques which introduce at least six additional transistors. The TG, DECAP and CSL techniques introduce the same number of additional transistors (four), but TG has higher power consumption because the transistors in TG are always active and are placed directly in the logic path. On

the other hand, DECAP approach results in lower power overhead because the transistors in cross-coupled arrangement consume less power. Similarly, the power consumption of the CSL configuration is lower because the added logic is floating.

5.4.3 Comparison of SET Mitigation Efficiency

A particular SET mitigation technique can be considered as efficient if it provides significant improvement of SET robustness with minimum area, delay and power overhead. The efficiency of SET mitigation techniques was quantified in [126] as the ratio between the decrease of SET pulse width and the increase of area. This metric was used to assess the efficiency of SET mitigation achieved by replacing a sensitive logic gate with alternative logic implementations. However, to the best of our knowledge, there is no a report on the comparison of SET mitigation efficiency of techniques analyzed in this work. In that regard, we introduce a generalized SET mitigation efficiency metric, denoted as *SME*,

$$SME (SET metric, overhead metric) = \frac{SET sensitivity metric change}{Overhead metric change}$$
(5.3)

In principle, *SME* denotes the ratio of the change of an SET sensitivity metric (critical charge, SER, generated SET pulse width or propagated SET pulse width) to the introduced area, delay or power overhead. Thus, there are multiple possible values of *SME* and this metric can be regarded as a function with two arguments – an SET metric and an overhead metric. The change of an SET sensitivity metric and the introduced overhead are calculated as the difference between respective values before and after the application of SET mitigation measures. For example, to assess the SET mitigation efficiency in relation to critical charge and area overhead, the corresponding *SME* function can be defined as,

$$SME (critical charge, area) = \frac{Increase of critical charge}{Increase of area}$$
(5.4)

Analogously, the *SME* function can be defined for other combinations of SET sensitivity metrics. For example, the SET mitigation efficiency in terms of the SET pulse filtering and introduced delay overhead can be expressed as,

$$SME (SET pulse width, delay) = \frac{Decrease of SET pulse width}{Increase of delay}$$
(5.5)

The *SME* function is an effective method for ranking the SET mitigation techniques in terms of their overall efficiency. Based on this figure of merit, the best technique for a particular circuit node can be selected. This implies that multiple *SME* values can be mapped to every logic gate and for every mitigation technique. For the sake of brevity, here we present the calculated *SME* values according to the relation (5.4). This relation allows to assess the contribution of a given technique to the improvement of SET robustness of a logic gate to direct particle strikes. In all cases the size factor x1 for the hardening techniques was considered. The obtained results are illustrated in Figure 5.19. Higher values of *SME (critical charge, area)* indicate better efficiency. As expected, the GU and GD are the most efficient for improving the SET

robustness to direct particle hits due to the large increase of critical charge. Interestingly, LU holds the third place and this mainly results from low area overhead. The difference in efficiency between CSL, TG, ST and DECAP techniques is relatively small, but DECAP has a slightly higher efficiency than CSL, TG and ST for all investigated gates. The GDMR was not considered in this case because the critical charge is not relevant for this technique.

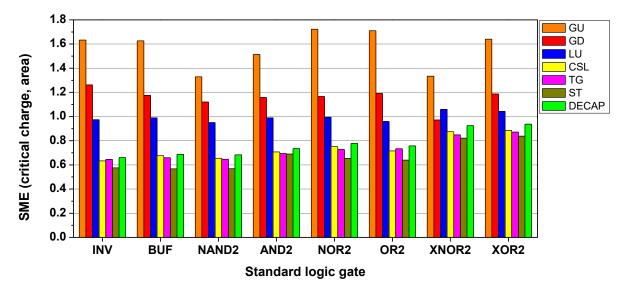


Figure 5.19: SET mitigation efficiency of hardening techniques considering the relation between critical charge and area overhead, for size factor x1 of hardening configurations (higher SME value is better)

5.5 Combined Application of Multiple SET Mitigation Techniques

Previous discussion has demonstrated the key advantages and disadvantages of the analyzed gate-level SET mitigation techniques. Each technique incurs the area, delay and power overhead, which need to be assessed with respect to the predefined area, delay and power constraints for a particular design. In addition, most techniques provide only limited improvement of the SET robustness. To compensate these limitations, it is imperative to combine multiple techniques, thus leveraging their complementary advantages and effectively minimizing the disadvantages of each technique.

In order to evaluate the combined use of multiple techniques, we have chosen the 10-gate NAND-NOR path analyzed in Section 5.3.5. As elaborated in Section 5.3.5, due to the propagation-induced pulse broadening effect, the SET pulse at the output may be broadened by more than 150 ps compared to the initial SET pulse. Thus, using the decoupling cells can provide limited suppression of the SET pulse by placing the x4 cells at two nodes in the path. Similarly, due to the limitations of each technique, any individual technique would not provide substantial SET suppression. As discussed in Section 5.3.5, the nodes 3 and 7 are most suitable for application of hardening measures. Therefore, these two nodes have been selected in this case as the target nodes for applying the SET filtering techniques. The gate upsizing has been chosen as the best option for mitigation of SET generation in the target node (node 1). To minimize the SET generation effects, the NAND2_x1 gate at the beginning of the path was replaced by NAND2_x2 gate. For SET filtering, different combinations of analyzed techniques have been investigated. The best

results in SET suppression have been achieved with the combinations involving the insertion of decoupling cells (DECAP), charge sharing logic (CSL), transmission gates (TG) and Schmitt trigger (TG) at nodes 3 and 7. In all cases the SET mitigation techniques have been applied with sizing factor x4.

In Figure 5.23, the output SET pulse width as a function of LET, for original path (without any hardening measures) and for path with applied hardening combinations, is presented. It can be seen that the largest SET suppression is achieved when GU is applied to node 1 and DECAP cells are applied to nodes 3 and 7. In this case, for the maximum investigated LET of 30 MeVcm²mg⁻¹, the SET pulse width at the output of logic path is reduced from 673 ps to 437 ps. Moreover, for LET below 2 MeVcm²mg⁻¹ the SETs are completely filtered, and for LET up to 5 MeVcm²mg⁻¹ the SET pulse width is reduced by more than 200 ps. Besides, the combination of TG with DECAP and CSL with DECAP also provide the reduction of SET pulse with by at least 200 ps. It is important to note that the aforementioned combinations provide larger SET suppression than using only the DECAP cells as in Section 5.2.

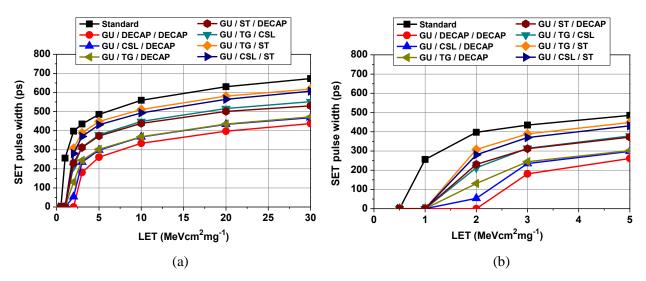


Figure 5.20: SET pulse width at the output of a 10-gate NAND-NOR path as a function of LET, for standard (non-hardened) path and for path with various combinations of mitigation techniques:
(a) for LET from 0.5 to 30 MeVcm²mg⁻¹, and (b) for LET from 0.5 to 5 MeVcm²mg⁻¹

In Table 5.12, the output SET pulse width for 30 MeVcm²mg⁻¹ and the propagation delay of the path without and with hardening is given. At the level of a single logic path, the delay overhead induced by the applied hardening logic is more critical than the area and power delay, because if the delay overhead violates the predefined delay constraints, the functionality of the entire circuit may be affected. It is thus necessary to select the hardening measures which introduce the lowest possible delay overhead. For the analyzed cases, the combination with the largest SET suppression (GU / DECAP / DECAP) introduces the delay of 660 ps, which is for 189 ps more than the original delay of the path. The minimum delay overhead is introduced by the combination of CSL and DECAP. It is important to note that the introduced delay is lower compared to the use of SET filtering with delay element and a guard gate. For example, the combination GU / DECAP / DECAP / DECAP can filter all SET pulses shorter than 400 ps with the delay overhead of 189 ps. To filter these SET pulses with a SET filter based on delay element and a guard gate, the introduced delay would be over 400 ps. This shows that the combined use of multiple techniques provides suppression of

short SETs with low delay overhead. Based on the SET pulse width and delay, the SET mitigation efficiency was calculated for each hardening combination, according to the relation (5.5), and the corresponding results are given in the third column in Table 5.12. As can be seen, the highest efficiency in SET mitigation can be achieved with the combination GU / DECAP / DECAP, which has the SME of 1.25.

Table 5.12: SET pulse width at the output of NAND-NOR path for $LET = 30 \text{ MeV cm}^2\text{mg}^{-1}$, propagation delay of the path without and with mitigation configurations, and corresponding SET mitigation efficiency SME (SET pulse width, delay)

Path configuration	Maximum SET pulse width (ps)	Propagation delay (ps)	SME
Standard (no hardening measures)	673	471	-
GU / DECAP / DECAP	437	660	1.25
GU / CSL / DECAP	468	657	1.1
GU / TG / DECAP	472	649	1.15
GU / ST / DECAP	530	771	0.48
GU / TG / CSL	552	652	0.67
GU / CSL / ST	607	732	0.25
GU / TG / ST	618	744	0.2

5.6 SET Mitigation in Standard Delay Cells

Based on the characterization results in Section 4.3.3.3, the standard cells with highest sensitivity to SETs are the standard delay cells (SDCs), with the SET pulses potentially longer than 1 ns. Therefore, mitigation of SETs in SDCs is particularly challenging. As the most suitable SET mitigation solution in this case, we have chosen two approaches based on duplication with a guard gate (GG): (i) complete duplication with a guard gate (SDC_CD), and (ii) partial duplication with a guard gate (SDC_PD). The SDC_CD and SDC_PD configuration are illustrated in Figure 5.21 and Figure 5.22, respectively. These duplication schemes are essentially the GDMR configuration. Thus, if an SET occurs in one gate replica, it will be masked by the GG. In SDC_CD design, the non-hardened SDC is duplicated and the outputs of two SDCs are connected to a GG. This approach can be applied to an existing SDC without modifying its design. On the other hand, in SDC_PD design, only the two most sensitive inverters in the cell (Inverters 2 and 3) are duplicated and connected to a GG. This approach requires to modify the existing cell structure. In both designs, an additional inverter (INV_X) is added together with GG.

The proposed hardened SDC configurations have been evaluated with the same simulation setup as in previous discussion. In Table 5.13, the SET pulse widths at the output of non-hardened SDCs, and the two hardened configurations (SDC_CD and SDC_PD), are presented. The analysis was done for two driving strengths of SDCs: SDC_x1 and SDC_x2. The output pulse width was observed for particle strikes in each inverter in the cell, and the GG and INV_X in the hardened versions. The presented results are for LET = $30 \text{ MeVcm}^2\text{mg}^{-1}$. It can be seen that the SDC_CD design completely masks all SETs occurring in internal inverters, and the GG and INV_X remain the only sensitive nodes. The SET pulse induced in the guard gate of SDC_CD is shorter than 700 ps for both cell designs. On the other hand, in the SDC_PD design the Inverters 1 and 4 (in SDC_x1) and the Inverter 4 (in SDC_x2) remain as vulnerable nodes. Nevertheless,

the main benefit of both duplication techniques is in eliminating the longest SETs that occur in the most sensitive nodes of SDCs. As a result, the contribution of SDCs to the overall SER would be reduced, since the electrical and timing masking factors are proportional to SET pulse width.

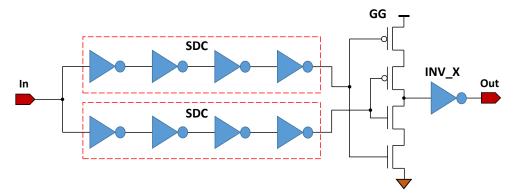


Figure 5.21: SET mitigation in standard delay cells with complete duplication

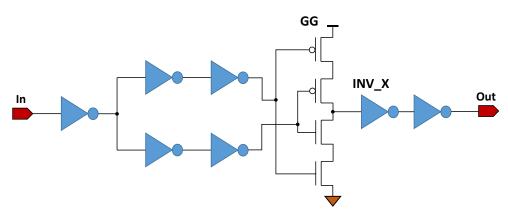


Figure 5.22: SET mitigation in standard delay cells with partial duplication

Table 5.13: SET pulse width at the output of standard delay cells, for standard version and two hardened
configurations (for low input level and $LET = 30 \text{ MeV cm}^2 \text{mg}^{-1}$)

G4 1	Output SET pulse width (ps)					
Strike location	SDC_x1			SDC_x2		
	SDC	SDC_CD	SDC_PD	SDC	SDC_CD	SDC_PD
Inverter 1	672	0	694	0	0	0
Inverter 2	772	0	0	1460	0	0
Inverter 3	806	0	0	1130	0	0
Inverter 4	483	0	487	474	0	512
GG	-	621	535	-	685	529
INV_X	-	495	495	-	495	495

To assess the effectiveness of the proposed SET mitigation solutions, it is necessary to evaluate the introduced area and delay overhead. The impact of power overhead would be less critical in a real complex design, and thus was not considered here. In Table 5.14, the normalized area and absolute delay for the original SDC_x1 and SDC_x2 designs, and the corresponding SDC_CD and SDC_PD configurations, are

given. SDC_PD introduces the area overhead up to 80 %, while for SDC_CD the area overhead is 115 %. Both solutions have relatively low delay overhead, as the delay increases for less than 250 ps compared to original SDC designs. However, SDC_CD has smaller delay overhead (9 % for SDC_x1 and 10.7 % for SDC_x2) compared to SDC_PD (33 % for SDC_x1 and 16 % for SDC_x2).

	SDC_x1		SDC_x2		
Cell type	Normalized cell area	Delay (ps)	Normalized cell area	Delay (ns)	
SDC	1	570	1	1.5	
SDC_CD	2.15	622	2.15	1.66	
SDC_PD	1.75	760	1.8	1.74	

Table 5.14: Normalized area and propagation delay for standard delay cells (SDC) with driving strength x1 and x2, and corresponding hardened configurations (SDC_CD and SDC_PD)

Although the presented hardening configurations for SDC do no provide total immunity to SETs, it must be noted that the alternatives such as TMR or SET filtering with delay element and guard gate are also not fully SET-immune. Namely, in both TMR and delay-based SET filtering the output nodes will be vulnerable to SETs. Thus, the solutions analyzed in this work provide significant improvement of SET robustness, with lower area overhead than TMR and lower delay overhead than delay-based SET filtering. Note that in the case of delay-based SET filtering the introduced delay overhead would be around 800 ps for SDC_x1 and around 1.4 ns for SDC_x2. Depending on the given design constraints, either SDC_PD or SDC_CD configurations can be used. If the area overhead is not critical and it is important to achieve minimum delay overhead, the SDC_CD configuration is more preferable than SDC_PD. Otherwise, when the area overhead is more critical than the delay overhead, the SDC_PD configuration is a better option.

5.7 Overall Comparison of SET Mitigation Techniques

The conducted analysis has confirmed that the gate-level SET mitigation techniques may provide a limited improvement in SET robustness at the cost of area, delay and power overhead. A common feature of all techniques based on insertion of redundant logic is that increase of the size of redundant logic provides better SET mitigation, but also increases the overheads. An important observation is that certain techniques may be more effective for certain gates than for others. The quantitative impact on the SET robustness improvement and the resulting overheads differ among the analyzed techniques. Thus, it is possible to rank the techniques in terms of the quantitative impact on the SET robustness improvement and the area, delay and power overhead. This can serve as a guideline for selecting an optimal combination of multiple approaches for a given design. Specifically, the following aspects need to be emphasized:

• The gate upsizing (GU) and gate duplication (GD) are superior over other techniques in terms of the enhancement of SET robustness to direct particle strikes, i.e. in terms of the increase of critical charge and reduction of SET pulse width. However, both GU and GD have weaker impact on SET filtering, whereby GD provides slightly better SET filtering.

- The gate duplication (GD) has very similar performance in terms of SET mitigation compared to GU. The two techniques are also similar in terms of delay overhead. However, the disadvantages of GD are higher area overhead (due to gate spacing and additional wires) and power overhead. Nevertheless, GD is a better option over GU in two cases. First, when high level of SET robustness is required, GD duplication can be applied to harden the gates for which higher drive strength is not available in the standard library. Second, GD provides better immunity to multiple strikes, and thus may be a better option if the introduced area overhead is permitted.
- The load upsizing (LU) has weaker impact on SET robustness improvement than other techniques, but on the other hand it introduces the lowest area, delay and power overheads. Thus, it could be a suitable choice for hardening the logic gates with very small critical charge, in cases where rigid design constraints do not permit the usage of techniques that introduce larger overhead. However, the impact of load on SET pulse width needs to be considered.
- The guarded dual modular redundancy (GDMR) enables to filter the SETs induced in the target gate, but the added guard gate and inverter are the main points of failure. This technique is especially suitable for filtering long SETs induced in certain logic gates. A good example are the standard delay cells, where the induced SET may be longer than 1 ns. As alternative to TMR or delay-based SET filtering, the use of GDMR can mitigate long SETs generated insider a target gate with acceptable delay overhead. However, the capability of GDMR to filter the incoming SETs is weaker compared to the techniques based on insertion of external logic. In addition, this approach introduces two additional sensitive nodes.
- The insertion of charge sharing logic (CSL) at the output of a logic gate introduces lower delay overhead than other techniques based on insertion of redundant logic. Therefore, this technique is the most appropriate choice when the delay constraints are rigid, e.g. for critical paths. Furthermore, the advantage of this techniques is that, due to the fact that the added logic is floating, a particle hit in the added logic will not cause observable SETs.
- The insertion of decoupling cells (DECAP) at the output of a logic gate has the advantage over LU, CSL, TG and ST in terms of higher rate of increase of critical charge with the size factor, and better efficiency in SET robustness improvement. In addition, this approach is effective in SET filtering in NAND2, AND2, XOR2, and XNOR2. This technique is a cost-effective alternative to techniques which induce higher overheads.
- The insertion of transmission gates (TG) at the output of a logic gate is appropriate option for SET filtering in BUF, AND2 and XOR2. It provides similar area overhead as CLS and DECAP, and lower area overhead than ST. On the other hand, TG incurs higher power overhead than DECAP and CSL, but lower power overhead than ST.
- The insertion of Schmitt trigger (ST) at the output of a logic gate provides better SET filtering than other techniques for INV, NAND2 and XOR2. However, this approach introduces very high area, delay and power overheads per gate, and is recommendable only if the area and delay constraints are not critical. Furthermore, this approach introduces two additional sensitive nodes (guard gate and inverter).

5.8 Summary

The results presented in this chapter has shown the promising potential of the proposed technique based on insertion of decoupling cells for SET mitigation in standard combinational gates. In addition, the proposed technique and the seven existing techniques have been characterized to determine their quantitative impact on the SET generation and propagation, and the introduced area, delay and power overheads. Obtained results can be used for constructing the characterization database of the SET mitigation configurations for each standard cell in a given library. In order to achieve this, the main directions for future work include:

- Verification: To verify the proposed SET hardening approach with decoupling cells on real circuits and under radiation exposure. This requires to first modify the layout of the existing decoupling cells by removing the default supply and ground connections, and thus forming a new standard cell that can be interfaced to other standard cells in a given design. Then, the test circuit composed of simple combinational chains with applied decoupling cells will be designed and tested under radiation to evaluate the impact of each technique on SET sensitivity.
- **SET sensitivity database formation**: To define an appropriate format for the characterization database for the gate-level SET hardening techniques that can provide full information on the impact of each technique on every gate, with respect to the SET robustness improvement and the introduced overhead. Moreover, it is essential to integrate the characterization results for hardening configurations with the SET database for the standard (non-hardened) cells into a unified SET database for a given digital library.
- **Optimization**: To establish an algorithm for selection of the most appropriate SET mitigation techniques for a given design, considering the quantitative effects of each technique specified in the characterization database.

Chapter 6

Particle Detection with Pulse Stretching Inverters

In order to reduce the SER of a complex design, the soft error mitigation techniques have to be applied at multiple abstraction levels. When the operating conditions and the system SER are variable, the use of both static and dynamic mitigation approaches is required to minimize the performance penalties. Generally, the gate- and circuit-level techniques are applied in a static manner to protect the most critical elements, while the system-level techniques are applied dynamically to maximize the radiation hardness under the critical radiation exposure. To enable the dynamic activation of soft error mitigation mechanisms, the on-line detection of particles that can cause the soft errors is mandatory. In this chapter, a particle detector based on the pulse stretching inverters, intended to serve as an on-chip trigger for the self-adaptive fault tolerance, is presented. The proposed solution allows for monitoring of particle flux and LET variations using lowcost purely digital processing logic. The following discussion is divided into eight sections. In Section 6.1, the motivation for particle detection in self-adaptive fault-tolerant systems is briefly reviewed. Section 6.2 describes the design and operation of pulse stretching inverters. Section 6.3 presents the simulation analysis of the normal response of pulse stretching inverters. In Section 6.4, the simulation analysis of the particle detection with pulse stretching inverters is presented. Section 6.5 introduces two conceptual designs of the processing logic for serial and parallel detector configurations. In Section 6.6, the comparison of proposed detector with existing solutions is given. An application scenario for the self-adaptive fault-tolerant system with the embedded particle detection is presented in Section 6.7. The main achievements and directions for future work are summarized in Section 6.8.

6.1 Introduction

In safety- and mission-critical applications executed in radiation environment, particularly in space environment characterized by complex and dynamic radiation conditions, the high performance electronics capable of real-time data processing with low power consumption and high robustness to ionizing radiation is required. However, such requirements are usually conflicting, and impose the need for design trade-offs. For example, the power consumption can be reduced by decreasing the supply voltage, but at the cost of increased susceptibility to soft errors. Alternatively, the soft error robustness of an electronic system can be enhanced by decreasing the operating frequency or increasing the supply voltage, but this on the other hand results in reduced performance and increased power consumption, respectively.

A widely accepted solution is in the use of adaptive multi- or many-core processing architectures, where the cores are dynamically configured into different operating modes according to the application requirements [55, 58]. By varying the number of cores engaged in parallel processing and powering off the unused ones, the optimal performance with minimal power overhead can be achieved. In a similar manner, the costeffective radiation hardening can be accomplished by applying the dynamic fault tolerance, e.g., by coupling the cores into N-modular redundant architectures (e.g., dual, triple and quadruple modular redundancy) under the high radiation levels (when the radiation exposure is high enough to affect the system's reliability). To enable the dynamic selection of operating modes during the runtime, the system must be equipped with sensors for monitoring the parameters and effects which influence the system's reliability (e.g., radiation intensity, temperature, supply voltage, clock frequency, aging). In this work, the focus is on detectors of energetic particles.

The use of dynamic soft error mitigation in space missions can be justified by the fact that the radiation exposure in space is variable, and the tasks performed by the space-borne electronics are changing during the mission. Thus, the reliability requirements in space missions may also vary under different operating scenarios. For example, the SPEs may lead to an increase of the particle flux in space by several orders of magnitude, and this condition can last for several hours or days. Accordingly, the SER of a target system will also increase several orders of magnitude due to its linear dependence on particle flux, according to the relation (2.3) (see Section 2.4.3). During the periods of intense radiation, the onboard electronics will be under increased danger of radiation-induced failures. In order to ensure timely detection of critical radiation levels and subsequently apply the fault-tolerant mechanisms, the real-time radiation monitoring is needed. As the soft errors represent the most critical radiation-induced threat in nanoscale CMOS technologies, it is essential to detect the energetic particles capable of causing these errors.

Since the particle flux is the most dominant radiation-related contributor to the SER of an electronic system, the continuous monitoring of flux variations during a space mission is essential for identification of the critical flux levels which can affect the system reliability. Besides measuring the particle flux, it is also important to measure the LET of detected particles. The value of LET gives important information on SET and SEU effects, which cannot be extracted only from the particle flux. Namely, the high-LET particles may cause long SETs and multiple SETs and SEUs, potentially increasing the system SER. Therefore, despite the fact that high-LET particles are less frequent in space compared to low-LET particles, their impact on system SER should be considered for accurate evaluation of the SER. Moreover, as the SETs are becoming an increasing threat for scaled technologies operating at low supply voltage and clock frequencies in the GHz range, it is crucial to provide the real-time monitoring of SET effects.

As alternative to the existing soft error (particle) detectors described in Section 3.5, this work introduces a solution based on the skewed inverter chains. The skewed logic has been traditionally used in high speed circuits due to the fast signal transitions, as well as in standard delay cells (see Section 4.3.3.3). A specific characteristic of skewed logic that can be exploited for detection of energetic particles is the pulse stretching feature [MA2]. For that reason, we use the expression "pulse stretching logic" instead of "skewed logic". The pulse stretching inverter chains have been used for experimental characterization of SET pulse width

in standard combinational cells [100], [MA7, MA8]. The role of pulse stretching inverters in that case is to extend the SET pulses induced in the standard combinational cells that are characterized, in order to ease their propagation through the subsequent processing logic. However, to the best of our knowledge, **the use of pulse stretching inverters as detectors of energetic particles has not been studied.**

We have investigated two detector configurations – serial and parallel connection of pulse stretching inverters [MA3, MA16, MA17]. It has been shown with extensive SPICE simulations that the serial configuration can be used to monitor the particle flux in terms of SET count rate, while the parallel configuration can monitor both the particle flux (in terms of SET count rate) and the LET variation (in terms of SET pulse width variation). Comparison with the existing solutions has shown that the proposed pulse stretching detector offers the following benefits: (i) *possibility to monitor both the flux and LET variations*, (ii) *low complexity and low power purely digital readout*, (iii) *possibility of integration into the target chip for insitu particle monitoring, (iv) immunity to false alarms and error accumulation*. Detailed description of the design and operation of the proposed particle detector based on pulse stretching inverters, with the emphasis of its advantages over the existing detectors in the context of self-adaptive fault-tolerant systems for space applications, is given in the following sections.

6.2 Design and Operation of a Pulse Stretching Cell (PSC)

The elementary pulse stretcher in CMOS technology can be realized with two cascaded custom-sized inverters as shown in Figure 6.1. In the following discussion, a two-inverter pulse stretcher will be denoted as the Pulse Stretching Cell (PSC). The transistor sizes for a PSC should be chosen such that for one inverter the channel width of PMOS transistor (W_{PMOS}) is smaller than that of NMOS transistor (W_{NMOS}), while for the other inverter the channel width of NMOS transistor is smaller than that of PMOS transistor. This ensures that an input pulse will be stretched as it propagates, whereby the pulse stretching (difference between input and output pulse widths) is defined by the PMOS-to-NMOS ratio. For the sake of simplicity, the PSC will be represented with a symbol depicted in Figure 6.2.

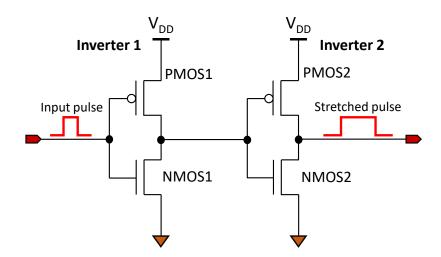


Figure 6.1: A two-inverter pulse stretching cell (PSC)



Figure 6.2: Symbol of two-inverter pulse stretching cell (PSC)

In general, for the fixed channel length L and for stretching the positive (0-to-1) pulses, the transistor sizes for a PSC can be defined with the following relations [MA2],

$$W_{NMOS1} = W_{PMOS2} \tag{6.1}$$

$$W_{PMOS1} = W_{NMOS2} \tag{6.2}$$

$$W_{NMOS1} > W_{PMOS1} \tag{6.3}$$

$$W_{PMOS2} > W_{NMOS2} \tag{6.4}$$

where W_{NMOS1} and W_{PMOS1} are channel widths of NMOS1 and PMOS1 transistors, while W_{NMOS2} and W_{PMOS2} are channel widths of NMOS2 and PMOS2 transistors. With transistor sizes according to relations (6.3) and (6.4), the negative (1-to-0) pulses will be suppressed. For stretching the negative pulses, the inequality signs in relations (6.3) and (6.4) have to be reversed.

The pulse stretcher expands the input pulse, i.e. increases its width, whereby the relation between the widths of the input and output pulses can be expressed in a general form as,

$$T_{OUT} = T_{IN} + \Delta T \tag{6.5}$$

where T_{OUT} denotes the width of the output pulse, T_{IN} is the width of the input pulse and ΔT is the pulse stretching of a single PSC, i.e. difference between the width of input and output pulses.

In general, the pulse stretching ΔT of a single PSC is directly proportional to the sizing ratio according to the relation,

$$\Delta T = a \cdot S \tag{6.6}$$

where S is the sizing ratio of a single PSC, and a is the proportionality factor which depends on the technology.

By cascading multiple PSCs, the stretching of input pulse can be increased. The output pulse width is linearly proportional to the number of cascaded stages, and for N cascaded stages the relation 6.5 can be rewritten as,

$$T_{OUT} = T_{IN} + b \cdot N \cdot \Delta T \tag{6.7}$$

The sizing ratio *S* of a single PSC is defined by the NMOS1-to-PMOS1 and PMOS2-to-NMOS2 channel width ratios, as follows,

$$S = \frac{W_{NMOS1}}{W_{PMOS1}} = \frac{W_{PMOS2}}{W_{NMOS2}}$$
(6.8)

According to the relation (6.8), the pulse width at the output of a PSC can be increased by using NMOS1 and PMOS2 transistors with larger channel widths. In general, the two inverters of a PSC can have different sizes and thus different sizing ratios. However, the transistors' maximum channel width is limited by design rules. Therefore, connecting multiple PSCs is a common approach when wide pulses are required. The pulse stretching can be also achieved by increasing the transistor' channel length. As will be shown in the following discussion, the use of multiple PSC stages and sizing of both channel width and length for all four transistors in a PSC is necessary to obtain high sensitivity for particle detection. Besides the transistor sizing, the operation of a PSC can be affected by a number of additional design, operating and technology parameters which must be considered.

6.3 Characterization of Normal Operation of PSC

Before analyzing the properties of PSC as a particle detector, it is important to assess its normal operation as a pulse stretcher. To this end, the response of a PSC was analyzed in terms of the *size ratio of PSC*, *supply voltage, temperature* and *number of cascaded PSCs*. It is worth to mention that the response of a PSC depends also on other parameters such as parasitic capacitances of interconnections, load size, process corners and transistors' size mismatch [MA2]. We have chosen in this case only the four aforementioned parameters because of their dominant impact on the normal response as well as on the SET sensitivity of the PSC [MA2].

The analysis was done with simulations in Cadence Spectre. As a case study, the IHP's 130 and 250 nm bulk CMOS technologies were chosen. In each simulation run, one parameter was varied over the specified range, while other parameters were kept at predefined (nominal) values. The simulation setup is illustrated in Figure 6.3.

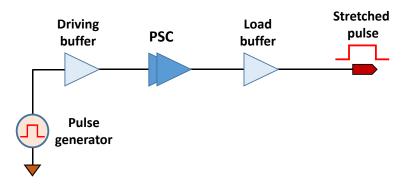


Figure 6.3: Simulation setup for analysis of normal operation of PSC

The input signal was a rectangular pulse with fixed duration of 100 ps, amplitude equal to the nominal supply voltage for the investigated technologies, and the rise and fall time constants of 10 ps each. Using different input pulse widths will result in different output pulse width according to the relation (6.5), but the pulse stretching will be the same.

To achieve realistic response, a buffer with minimum driving strength was inserted between the pulse source and the input of PSC, and the same buffer size was used as a load. To obtain comparable results, the same ratios between channel width W and channel length L for individual transistors were used for both technologies. The channel lengths are $0.24 \,\mu m$ (for 250 nm) and $0.13 \,\mu m$ (for 130 nm), whereas the nominal supply voltages are 2.5 V (for 250 nm) and 1.2 V (for 130 nm).

6.3.1 Impact of Technology

In Figure 6.4, the waveforms of the input pulse and the stretched pulses at the outputs of first and second inverter in the PSC are illustrated. For both technologies the same sizing ratio S = 10 was used. It can be observed that significant pulse stretching occurs after the pulse passes through each inverter. In addition, the pulse stretching differs for the two analyzed technologies. The input pulse for 250 nm technology is stretched by 292 ps (from 100 ps to 392 ps), while for 130 nm technology the input pulse is stretched by 245 ps (from 100 ps to 345 ps). This indicates that a detailed characterization is needed for every technology in order to determine the parameters *a* and *b* in relations (6.6) and (6.7).

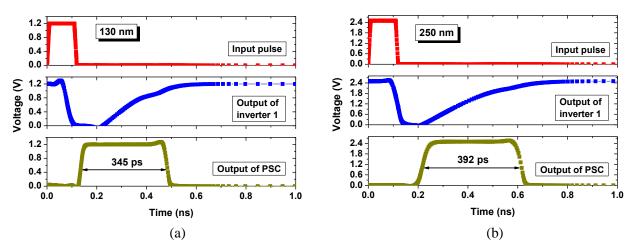


Figure 6.4: Stretching of 100 ps pulse with a single PSC in: (a) 130 nm, and (b) 250 nm technology

6.3.2 Impact of Transistor Sizing

Based on the relations (6.5) - (6.8), for a given technology the response of the PSC is predominantly influenced by the transistor sizing. To demonstrate this, two sizing configurations have been analyzed: (i) increasing of sizing ratio *S* from 5 to 15, and (ii) upsizing of all transistors for fixed sizing ratio *S* = 5.

Figure 6.5 (a) illustrates the impact of sizing ratio *S* on the output pulse width. The sizing ratio was varied by increasing successively the channel widths of NMOS1 and PMOS2 transistors, while the channel widths of PMOS1 and NMOS2 transistors were kept constant. The output pulse width increases linearly with the sizing ratio in accordance with the relations (6.5) and (6.6), and the slope of this relation depends

on technology. Thus, by fitting the dependence illustrated in Figure 6.5 (a), the parameter a in relation (6.6) can be determined for each technology. Simulations for different input pulse widths have shown that the absolute increase of the output pulse width is the same for all input pulse widths.

The effect of upsizing of all transistors in the PSC, for constant sizing ratio S = 5 and for the same *W/L* ratio for both technologies, is depicted in Figure 6.5 (b). The channel widths of PMOS1 (NMOS2) and NMOS1 (PMOS2) transistors have been varied equally to maintain the predefined sizing ratio. For both investigated technologies, this upsizing approach does not result in significant variation of the output pulse width. A minor decrease of the output pulse width was observed for both technologies, when all transistors are upsized, and this decrease is slightly larger for 130 nm technology.

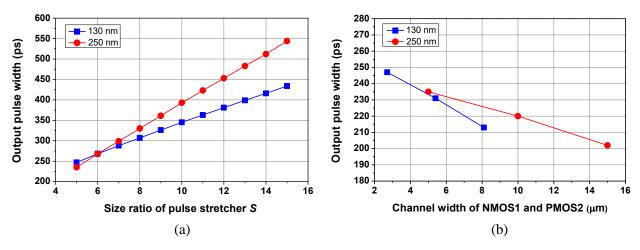


Figure 6.5: Output pulse width as a function of: (a) size factor S, (b) transistor size (for S = 5)

6.3.3 Impact of Supply Voltage and Temperature

Figure 6.6 (a) illustrates the dependence of PSC's output pulse width on supply voltage. The supply voltage was varied from -10% to +10% with respect to nominal values, because this is the normal operating range for digital logic in investigated technologies. The sizing ratio of PSC was S = 5 for both technologies. It can be observed that the reduction of supply voltage leads to a moderate increase of the output pulse width, whereby this increase is around 25 ps for 250 nm technology and 50 ps for 130 nm technology over the investigated supply voltage range. The increase of output pulse width is related to the increase of low-to-high and high-to-low transition times with the reduction of supply voltage.

The dependence of the output pulse width on temperature is depicted in Figure 6.6 (b). The temperature was varied from -40 to 125 °*C* to cover the typical operating conditions encountered in harsh environments such as space. In all simulations the sizing factor of pulse stretcher was S = 5, and the analysis was conducted with the input pulse width of 100 ps. For both technologies, the temperature increase up 80 °C causes slight increase of the output pulse width, and for temperatures beyond 80 °C the output pulse width saturates. The impact of temperature is stronger for 130 nm technology. Observed variation of the output pulse width can be attributed to the increase of transistors' switching speed (transition times) with temperature. Simulations have been performed for sizing factors S > 5, and it was observed that for higher sizing factors the variation of output pulse due to temperature is more pronounced.

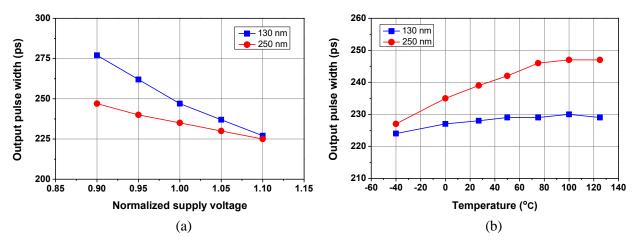


Figure 6.6: Output pulse width as a function of: (a) normalized supply voltage, (b) temperature

6.3.4 Impact of the Number of Cascaded Pulse Stretchers

As the pulse stretching with a single PSC is limited by transistor sizes, wider pulses (e.g. in the range of ns) can be obtained by cascading multiple PSCs. A configuration composed of 10 cascaded PSCs has been analyzed. In Figure 6.7, the pulse width at the output of even PSC stages is depicted. The output pulse width increases linearly with the number of cascaded pulse stretching stages, for both technologies. Moreover, the pulse stretching strongly depends on the technology. Therefore, by fitting the simulation results, the value of parameter b in relation (6.7) can be obtained for each technology. Comparing with the results in Figure 6.7 shows that cascading multiple PSCs is more effective than transistor upsizing when it is required to obtain larger pulse stretching.

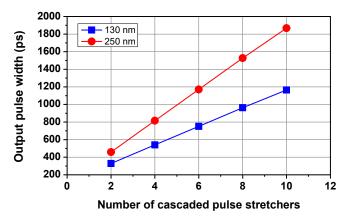


Figure 6.7: Output pulse width as a function of the number of cascaded pulse stretchers

6.4 Characterization of PSC as a Particle Detector

The pulse stretching feature of a custom-sized PSC, demonstrated in previous section, can be leveraged for detection of energetic particles responsible for the soft errors. As the CMOS circuits are inherently sensitive to SETs, the particle strike on a sensitive (off-state) transistor in the pulse stretcher may result in an SET pulse. The main benefit of pulse stretching is that it can potentially provide high sensitivity to particle

strikes, because the transistor sizes can be adjusted to enable the formation of sufficiently long SETs which can then propagate through the subsequent processing logic. As a result of pulse stretching, even very lowenergy (low-LET) particles may cause observable SETs. This property qualifies the PSC as a promising candidate for particle detection.

However, to act as a particle detector in self-adaptive fault-tolerant applications, the PSC must satisfy the following basic requirements:

- (i) Sensitive area should be as large as possible in order to maximize the probability of particle strikes,
- Sensitivity of individual inverters to particle strikes should be higher than that of standard cells used in the design of the target system,
- (iii) Inverters in a PSC should have the same or similar detection threshold, i.e. the same or similar critical charge (or LET_{TH}),
- (iv) Induced SET pulse should be wide enough so that it can be detected and processed by the subsequent processing logic.

To use the PSC as a particle detector, the input must be set to fixed logic level. By setting either low or high input level, one transistor in each inverter will always be in the off-state and thus will be sensitive to particle strikes. Following the relations (6.1) - (6.4), we have chosen low input level, as illustrated in Figure 6.8. This means that NMOS1 and PMOS2 will be the off-state transistors, while PMOS1 and NMOS2 will be the on-state transistors. By increasing the size of off-state transistors, according to the relations (6.3) and (6.4), the probability of particle strike will be increased. On the other hand, the on-state transistors act as restoring elements, providing the current to compensate the induced charge. As the drive current of restoring transistors is proportional to their W/L ratio, smaller channel widths of on-state transistors may be increased to further enhance the SET sensitivity. Therefore, applying these guidelines for PSC sizing ensures that the requirements (ii) and (iii) are met.

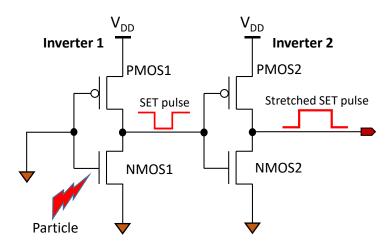


Figure 6.8: SET response of PSC due to a particle strike in off-state NMOS transistor

Using a single PSC as a particle detector is not practical due to small sensing area. In order to increase the overall sensitive area and satisfy the requirement (i) given above, multiple PSCs must be connected either in parallel or in series. The serial connection can be achieved by using either a single long chain of PSCs or shorter PSC chains connected with the OR-tree to obtain a single output. Alternatively, multiple PSCs can be connected in parallel array and then a number of such arrays can be connected with OR-tree. In any case, the transistor sizes and chain/array lengths should be selected such that the particle strike in any PSC results in an observable output pulse. An even number of inverters per chain is required to ensure the same polarity of the SET pulse at the output of the chain regardless of the strike location.

Regarding the aforementioned requirement (iv), it must be ensured that for any deposited charge exceeding the critical charge (or LET_{TH}), the SET pulse width at the output of the detector is sufficient to trigger the subsequent processing logic. To achieve this, the sizing of inverters in the PSC and the number of PSCs in serial or parallel configuration must be carefully selected in the design phase. In general, the width of the SET pulse at the output of the detector should be at least twice the propagation delay of the subsequent logic gates in the processing unit so that it can propagate without significant attenuation. Thus, the width of at least several hundred picoseconds can be considered as the minimum required width.

Besides the aforementioned requirements (i) - (iv), the PSC-based particle detector together with the accompanying readout logic must also satisfy the following criteria for application in the self-adaptive fault-tolerant systems:

- (a) possibility to detect both particle flux and LET
- (b) immunity to false alarms
- (c) low detection latency (fast response)
- (d) simple and low-cost processing logic
- (e) low area, power and performance overhead
- (f) possibility to be integrated on the same chip with the target system

As elaborated in Section 3.5, there is no any existing particle detector which amalgamates all above mentioned criteria. We aim to demonstrate that the proposed detector based on pulse stretching inverters can meet to a large extent these criteria, offering a competitive alternative to the state-of-the-art solutions. To this end, the simulation analysis of the SET sensitivity of a single PSC, as well as serial and parallel PSC configurations, is presented in the following.

6.4.1 SET Effects in a Single PSC

As the single PSC serves as a fundamental sensing element in the proposed particle detector, it is important to first investigate its SET response. The analysis was done through extensive simulations with Cadence Spectre, using the setup illustrated in Figure 6.9. Without loss of generality, the analysis was done only for the IHP 130 nm technology. Based on the analysis of the normal response presented in previous section, it can be expected that the results for 250 nm technology would be qualitatively similar, and only the quantitative contribution of different parameters would vary. For simulation of SETs, the standard current injection approach with the bias-dependent current source [205] was applied. The timing parameters of the current pulse were fixed (rise time = 10 ps and fall time = 100 ps).

The SET sensitivity of a single PSC was characterized by analyzing the dependence of LET_{TH} and SET pulse width on: (i) PSC sizing, (ii) supply voltage, (iii) temperature, and (iv) LET. It is important to mention that the SET response of the PSC depends on additional parameters, like the normal response. Considering that the PSCs would be placed at close proximity on the chip to obtain as large detection area as possible, the impact of the parasitic capacitances of interconnections would be minor, and therefore it has been neglected in this analysis. Similarly, due to their lower impact on the SET sensitivity as shown in [MA5], the load size, process variations and transistor size mismatch have not been considered.

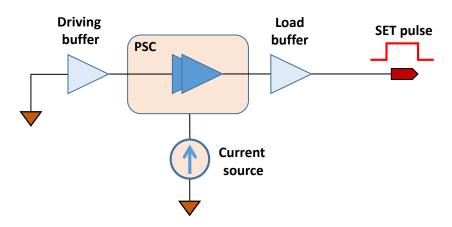


Figure 6.9: Simulation setup for analysis of SET response of PSC

6.4.1.1 Impact of PSC Sizing

As elaborated in previous discussion, transistor sizing is a key design technique for tuning the sensitivity of PSC to SETs. In order to select the transistor sizes (channel widths and lengths) that provide the lowest possible detection threshold (lowest LET_{TH}), the dependence of LET_{TH} on transistor sizes of both inverters in the PSC was analyzed. The current was injected successively at the output of each inverter, and LET was varied to obtain the minimum value (LET_{TH}) which results in an SET pulse at the output of PSC. The simulation results are illustrated in Figures 6.10 and 6.11.

Because LET_{TH} decreases with the increase of the channel width of on-state transistors PMOS1 and NMOS2, it is necessary to choose the minimum possible channel widths. For the investigated 130 nm technology, the minimum channel width is limited to 150 nm by design rules. With the selected channel width of 150 nm for PMOS1 and NMOS2 transistors, the SET sensitivity was analyzed by varying their channel lengths from 130 nm to 1 μ m. As depicted in Figure 6.10, by increasing the channel length of on-state transistors, the detection threshold (LET_{TH}) of both inverters is reduced, i.e., the SET sensitivity of the PSC is increased. On the other hand, for off-state transistors the minimum possible channel length of 130 nm was chosen, and then the LET_{TH} was analyzed in terms of their channel width. As shown in Figure 6.11, by decreasing the channel width of NMOS1 and PMOS2, the detection threshold (LET_{TH}) decreases. Therefore, the illustrated dependences of LET_{TH} on transistor sizes can serve as the basis for selection of the optimal channel widths and lengths for a PSC, as will be described in the following section. Notice that the transistor sizes for PSC differ from those for the skew-sized inverters in standard delay cells analyzed in Section 4.3.3.3.

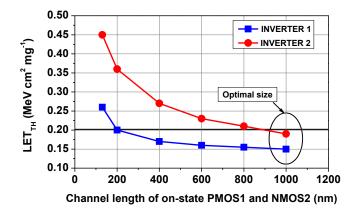


Figure 6.10: Dependence of LET_{TH} on channel length of on-state transistors (PMOS1 and NMOS2)

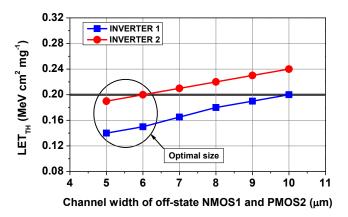


Figure 6.11: Dependence of LET_{TH} on channel width of off-state transistors (NMOS1 and PMOS2)

6.4.1.2 Selection of Optimal Transistor Sizes for PSC

As one of the main requirements for the particle detector is to have higher sensitivity than the target system, the SET and SEU sensitivity of the standard cells should be used as a reference in the selection of transistor sizes for the PSC. The LET_{TH} values of 6T SRAM cell, D flip-flop and combinational cells characterized in Sections 4.3 and 4.4, are given in Table 6.1. For combinational cells, only the minimum LET_{TH} values and the corresponding input levels are given.

Based on the results in Figures 6.10 and 6.11, the optimal size for the PSC is: W/L =150nm/1 μ m (for PMOS1 and NMOS2) and W/L = 6 μ m/130nm (for NMOS1 and PMOS2). With these transistor sizes, the LET_{TH} is less than 0.2 MeVcm²mg⁻¹, which is lower than that of all standard cells in Table 6.1. Note that the PSC is also more sensitive than the 6T SRAM cell. This suggests that the particle detector based on PSC would potentially be more sensitive that the SRAM-based detectors. It is important to mention that according to Figure 6.11, the optimal size for the channel width of off-state transistors NMOS1 and PMOS2 is 5 μ m. However, we have chosen 6 μ m to achieve larger sensing area, while maintaining the LET_{TH} below 0.2 MeVcm²mg⁻¹. Nevertheless, these values can be modified according to the application requirements and design constraints, without significantly degrading the sensitivity. For practical applications it is imperative that the detector can sense a wide range of energetic particles occurring in the real radiation environments, particularly the low-LET particles which are abundant in natural radiation environments

such as space. Since the LET of real energetic particles is usually greater than 1 MeVcm²mg⁻¹, the PSC with the LET_{TH} below 1 MeVcm²mg⁻¹ will be capable of detecting most energetic particles.

Target cell	LET _{TH} (MeVcm ² mg ⁻¹)
6T SRAM	0.28 (stored 0) / 0.2 (stored 1)
D flip-flop	0.52
INV	0.42 (for input = 0)
BUF	0.45 (for input = 1)
NAND	0.41 (for input = 01)
AND	0.42 (for input = 11)
NOR	0.27 (for input = 00)
OR	0.41 (for input = 11)
XOR	0.27 (for input = 01)
XNOR	0.29 (for input = 01)

Table 6.1: LET_{TH} for standard logic cells and SRAM cell in IHP's 130 nm technology

6.4.1.3 Impact of LET

Once the transistor sizes for the PSC are chosen, the output SET pulse width at fixed supply voltage and temperature will mostly depend on the particle LET. To investigate this dependence, the simulations were done for a range of LET from 1 to 30 MeVcm²mg⁻¹, using the transistor sizes proposed in previous section. The nominal supply voltage (1.2 V) and temperature of 27 °C were used in simulations. The pulse width at the output of PSC in terms of LET, for current injection in both inverters, is illustrated in Figure 6.12. As can be seen, the increase of LET results in the monotonic increase of SET pulse width. For the investigated LET range, the SET pulse width varies from 487 ps to 4.16 ns. For strikes in Inverter 1, the SET pulse width varies from 3.7 to 4.16 ns, while for strikes in Inverter 2, the SET pulse width is from 487 to 986 ps. The change of SET pulse width is almost the same for both inverters, but longer SETs are obtained for strikes in Inverter 1 because of additional pulse stretching due to the propagation through Inverter 2.

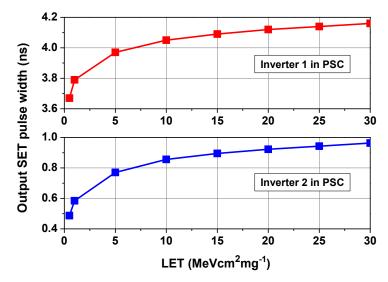


Figure 6.12: Output pulse width of a single PSC as a function of LET

6.4.1.4 Impact of Supply Voltage

The dependence of LET_{TH} on supply voltage is illustrated in Figure 6.13. Because the driving strength of restoring transistors decreases with the decrease of supply voltage, the LET_{TH} of both inverters in the PSC also decreases with supply voltage. This indicates that the supply voltage can be exploited as a means for controlling the detection threshold of PSC. Furthermore, the combination of transistor sizing and supply voltage adjustment can be used to tune the PSC's sensitivity in the design phase. It should be noted that the supply voltage variations would produce strong impact on the SET sensitivity of the PSC SET pulse width, as will be shown in the following discussion.

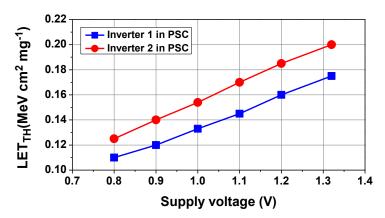


Figure 6.13: LET_{TH} for two inverters in a single PSC as a function of supply voltage

6.4.1.5 Impact of Temperature

Figure 6.14 depicts the variation of LET_{TH} when temperature is varied from -40 to 125 °C. Higher temperatures result in the decrease of LET_{TH}, and this is related to the reduction of transistors' driving current due to the reduction of carrier mobility. It can be noticed that the impact of temperature is weaker compared to that of supply voltage. Namely, LET_{TH} varies by approximately 0.04 MeVcm²mg⁻¹ over the investigated temperature range, and by almost 0.08 MeVcm²mg⁻¹ over the supply voltage range. The detection threshold of the PSC would not be degraded by temperature variations in the investigated range. However, like with the supply voltage, the temperature variations could significantly influence the SET pulse width response, as will be demonstrated in the following.

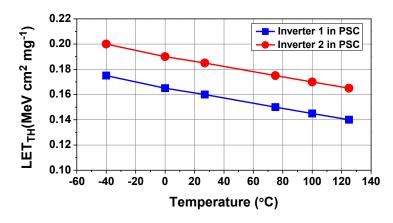


Figure 6.14: LET_{TH} for two inverters in a single PSC as a function of temperature

6.4.2 SET Effects in PSCs Connected in Series

A general structure of a serial PSC configuration is illustrated in Figure 6.15. The input of first PSC is grounded, while the output is routed to the processing logic. Thus, an SET induced in any PSC will propagate to the output, and the number of captured SETs is proportional to the particle flux. To investigate the SET effects in a serial PSC chain, the same transistor sizes and the simulation setup as in previous Section have been applied. In this study, a 10-PSC (20-inverter) configuration is analyzed.

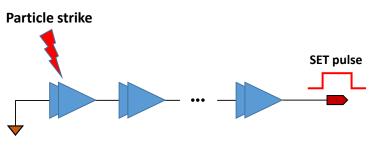


Figure 6.15: Serial PSC configuration

6.4.2.1 Impact of Chain Length

The LET_{TH} for each inverter in the chain and the corresponding output SET pulse width have been analyzed by injecting the current pulse successively in each inverter. The results are presented in Figure 6.16. As can be seen, the LET_{TH} values of individual inverters are almost constant, which is a desired feature because ideally all elements in the detector chain should have the same sensitivity to particle strikes. Due to the stretching feature of the PSC chain, the output SET pulse width for LET = LET_{TH} increases linearly as the target inverter is at larger distance from the output. The minimum SET pulse width of 320 ps is obtained when the current is injected in the last inverter, while the maximum SET pulse width of around 36 ns is obtained for the current injection in the first inverter. The pulse width of 360 ps is sufficient to propagate further to the processing logic, since the propagation delay of standard logic cells in the analyzed 130 nm technology is below 100 ps. It is noteworthy to mention that by increasing the number of inverters in the chain up 100, the output SET pulse width for LET = LET_{TH} will increase linearly up to 164 ns, and for longer chains the SET pulse width will be in the range of μ s. This should be taken into account in the design of the processing circuit, because long SET pulses result in high latency.

6.4.2.2 Impact of LET

To evaluate the impact of LET on the SET pulse width at the output of PSC chain, the same current injection approach as in previous Section was applied. The dependence of the output SET pulse width, when the current is injected in first and last inverters in the chain, is shown in Figure 6.17. As can be noticed, the SET pulse width increases gradually with LET, and then eventually saturates at certain LET value. The output SET pulse width and the start of saturation region depend on the strike location, i.e. on the inverter which is hit. The saturation region is wider when the target inverter is at larger distance from the output. For example, when the current is injected in first inverter in the chain, the output SET pulse width saturates already at LET of around 0.5 MeVcm²mg⁻¹. It was observed that the SET pulse width saturates at LET < $0.5 \text{ MeVcm}^2\text{mg}^{-1}$ for the first ten inverters in the chain. Because of pulse width saturation, it would be

impossible to differentiate the LET values in the saturation region based on the SET pulse width, and hence the serial PSC chain is not suitable for measuring the LET variations.

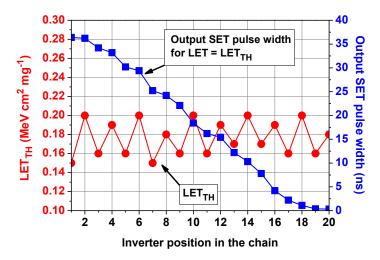


Figure 6.16: LET_{TH} and corresponding output SET pulse width when current pulse is successively injected in each inverter in a chain composed of 20 pulse stretching inverters (10 PSCs)

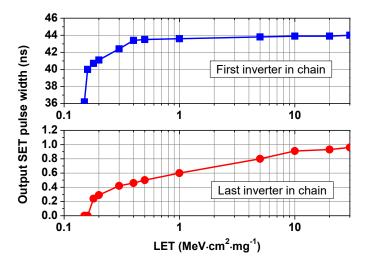


Figure 6.17: Output SET pulse width as a function of LET, when the current pulse is injected in the first and last inverters of a chain composed of 20 pulse stretching inverters (10 PSCs)

6.4.2.3 Impact of Single Event Double Transients

An important issue for any particle detector are the multiple SETs or SEUs caused by a single particle strike, which can result in erroneous SET or SEU counts. Due to the chosen transistor sizes for PSC, we estimate that a single particle can hit simultaneously a maximum of two inverters. Thus, for the proposed detector, the Single Event Double Transients are relevant. We have evaluated the effect of Single Event Double Transients in a 20-inverter pulse stretching chain by injecting two current pulses simultaneously in all adjacent inverter pairs. A sample of results is illustrated in Figure 6.18. In all investigated cases the two simultaneous SETs were overlapping and resulted in a single pulse at the output of the chain. This is due to the low propagation delay of individual inverters and the stretching of the SET pulse. The only consequence

of double SETs is the increase of the output SET pulse width. This implies that the proposed inverter chain is inherently robust to double SETs and is thus immune to erroneous SET counts.

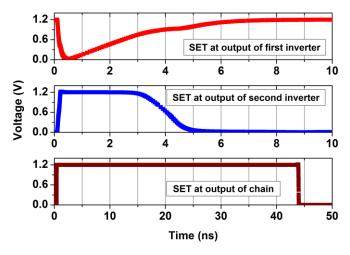


Figure 6.18: SET response due to simultaneous current injection in two inverters of a 20-inverter pulse stretching chain

6.4.2.4 Impact of Supply Voltage

The dependence of the output SET pulse width on supply voltage, when the current is injected successively in the first and last inverters of a 20-inverter pulse stretching chain, is shown in Figure 6.19. The analysis was done for LET of 10 MeVcm²mg⁻¹, and supply voltage from 0.8 V (minimum supply voltage) to 1.2 V (nominal supply voltage). The SET pulse width increases by more than 50 % as supply voltage is reduced from 1.2 to 0.8 V. It was observed that supply voltage variations have strongest impact on the SET pulse width when the strike occurs in the first inverter in the chain, and this impact gradually diminishes as the target inverter is closer to the output. This indicates that the skew sizing enhances the sensitivity of a PSC chain to supply voltage variations.

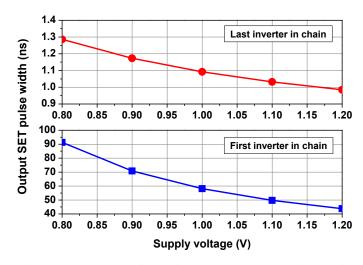


Figure 6.19: SET pulse width at the output of a 20-inverter pulse stretching chain, as a function of supply voltage, for LET = $10 \text{ MeV cm}^2\text{mg}^{-1}$ and temperature of 27 °C

6.4.2.5 Impact of Temperature

Figure 6.20 illustrates the SET pulse width at the output of a 20-inverter pulse stretching chain as a function of temperature, when the current is injected successively in the first and last inverters in the chain, for LET of 1 MeVcm²mg⁻¹. As can be observed, at higher temperatures the SET pulse is wider. However, the impact of temperature is weaker compared to supply voltage, causing a maximum of 35 % change of the SET pulse width. It is particularly important to note that the temperature variations have significantly stronger impact on SETs induced in Inverter 1, as the SET pulse width increases by almost 1.5 ns when temperature increases from 27 to 125 °C. Thus, as in the case of supply voltage, the skew sizing also has strong impact on the temperature dependence of the SET response of a PSC chain.

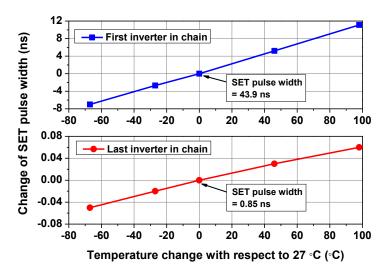


Figure 6.20: Change of SET pulse width at the output of a 20-inverter pulse stretching chain, as a function of temperature, for LET = $10 \text{ MeV cm}^2\text{mg}^{-1}$ and supply voltage of 1.2 V

6.4.3 SET Effects in PSCs Connected in Parallel

Because the serial PSC configuration is insufficiently sensitive to LET variations, as shown in Section 6.4.2, we have investigated the parallel connection of PSCs as a possible solution for simultaneous measurement of particle flux and LET variations. By measuring both the particle flux and LET, the radiation intensity can be estimated more accurately. The idea of parallel PSC configuration is to measure the LET variations in terms of the SET pulse width variations, while the flux is measured in terms of the SET count rate (in the same way as with the serial PSC configuration). The PSCs are configured in a parallel array by connecting the inputs of all PSCs to low logic level (ground) and connecting all outputs together to obtain a single output terminal, as shown in Figure 6.21. Hence, a particle strike in the sensitive transistor of any PSC will produce an SET pulse at the output, which then propagates to the subsequent processing logic. The captured SET pulses are processed to determine the SET count rate and the SET pulse width variation. To alleviate the SET pulse width saturation effect observed with the serial PSC configuration, in this case only one PSC is connected between the input and output. The sensitive area of the complete detector can be tuned by selecting the appropriate number of parallel arrays connected with an OR-tree. Thus, it is important to investigate how the number of parallel cells affects the SET sensitivity of an array, particularly in the

context of increasing the load with the number of PSCs. The exhaustive circuit simulations have been performed to investigate the SET response of a parallel PSC array in terms of: (i) size of transistors in the PSC, (ii) number of PSCs connected in parallel, (iii) particle LET, (iv) supply voltage, and (v) temperature.

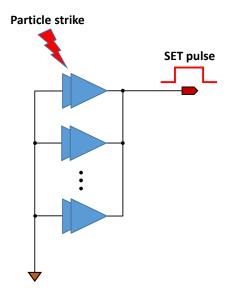


Figure 6.21: Parallel PSC configuration

6.4.3.1 Impact of PSC Sizing

The parallel PSC configuration can be designed with the same transistor sizes as those chosen for the serial PSC chain. However, these sizes would limit the SET sensitivity because of the loading effect. Namely, in parallel PSC configuration, the second inverter in each PSC will have larger load because its output is connected to outputs of all other PSCs. As a result, the SET sensitivity of the second inverter in each PSC will decrease with the increase of the number of PSC. Hence, it is necessary to choose the optimal transistor sizes which provide the highest possible SET sensitivity of both inverters in each PSC, for the parallel array composed of as many PSCs as possible. To ensure that a particle strike in any sensitive transistor in the PSC array will result in an observable SET pulse, both inverters in the PSC should have the threshold LET, LET_{TH} , below the LET of real energetic particles that can be encountered in a target radiation environment. The LET of most energetic particles in space is greater than 1 MeVcm²mg⁻¹. For example, one of the heavy ions with lowest LET is He² (LET = 1.2 MeVcm²mg⁻¹). Therefore, we define the LET of 1 MeVcm²mg⁻¹ as the desired detection threshold for the parallel PSC configuration.

In Table 6.2, the chosen channel widths and lengths for both transistors in a single PSC are given. The main difference with respect to the serial PSC configuration is that the channel length of NMOS transistor in Inverter 2, L_{NMOS2} , is increased from 1 to 6 µm. This was done in order to compensate for the loss in sensitivity when multiple PSCs are connected in parallel. Namely, as the number of PSCs in parallel increases, the load capacitance at the output of Inverter 2 will increase and consequently its threshold LET will also increase. The chosen transistor sizes have been selected for the array of 12 PSCs connected in parallel, and enable to detect the SET pulses induced by LETs below 1 MeVcm²mg⁻¹. In the following we will described the reason for choosing 12 PSCs in parallel as the optimal size for a PSC array.

When multiple PSCs are connected in parallel, the threshold LET of individual PSCs may change. To investigate this, the simulations have been done for different number of PSCs in parallel, and the results are shown in Figure 6.22. The results have been obtained for nominal supply voltage of 1.2 V and temperature of 27 °C. Because all PSCs have the same sizing, it is sufficient to inject the current pulse in one PSC. As can be seen, when the number of PSC increases from 1 to 12, the threshold LET of Inverter 1 changes very little, from 0.27 to 0.36 MeVcm²mg⁻¹. That is because the load for Inverter 1 is the same regardless of the number of PSCs connected in parallel. On the other hand, the threshold LET of Inverter 2 increases linearly from 0.11 to 0.96 MeVcm²mg⁻¹. This increase of threshold LET is the result of linear increase of load capacitance with the increase of the number of PSCs in parallel. As can be observed, by comparing Figure 6.22 with the results in Table 6.1, Inverter 1 in PSC has lower threshold LET than most standard cells. However, Inverter 2 has higher threshold LET than all presented cells when more than 4 PSCs are connected in parallel. Nevertheless, the LET lower than 2 MeVcm²mg⁻¹ can hardly cause an SET pulse that can propagate through a typical combinational chain in 130 nm technology. Thus, the parallel PSC configuration with the proposed sizing has a potential to detect the critical radiation exposure.

Inverter in PSC	Channel width and length		
Inverter 1	$W_{PMOS1} = 150 \text{ nm}, L_{PMOS1} = 1 \ \mu m$ $W_{NMOS1} = 6 \ \mu m, L_{NMOS1} = 130 \ nm$		
Inverter 2	$W_{PMOS2} = 6 \ \mu m, \ L_{PMOS2} = 130 \ nm$ $W_{NMOS2} = 150 \ nm, \ L_{NMOS2} = 6 \ \mu m$		

Table 6.2: Transistor sizes for parallel PSC configuration

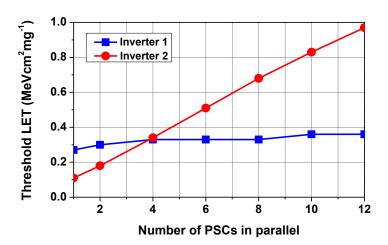


Figure 6.22: Threshold LET of Inverter 1 and Inverter 2 in a PSC, for different number of PSCs

6.4.3.2 Impact of the Number of PSCs and Particle LET

Besides the threshold LET, the dependence of the output SET pulse width on the number of PSCs and the particle LET is important for selection of the optimal number of PSCs that can be connected in parallel. The SET response for both inverters in a PSC, for the nominal supply voltage of 1.2 V and nominal temperature of 27 °C, is illustrated in Figures 6.23 and 6.24.

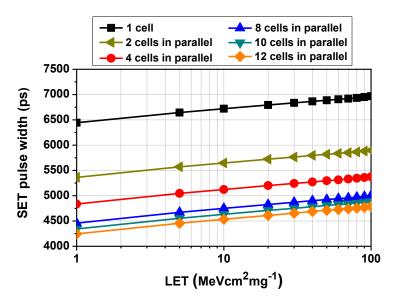


Figure 6.23: SET pulse width as a function of LET and number of cells connected in parallel, when the current pulse is injected in first inverter in PSC

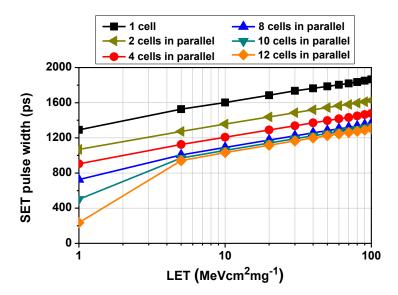


Figure 6.24: SET pulse width as a function of LET and number of cells connected in parallel, when the current pulse is injected in second inverter in PSC

As can be observed, the output SET pulse width increases logarithmically with LET, but this dependence appears linear due to the log-scale on x-axis. By increasing the number of cells connected in parallel, the load capacitance for each cell increases, and consequently the output SET pulse width decreases. For both inverters in each PSC, the SET pulse width increases by almost 550 ps in the LET range from 1 to 100 MeVcm²mg⁻¹. Note that this LET range covers most of the particles that can cause soft errors in space. For strikes in the first inverter in PSC the output pulse width is between 4 and 7 ns, while for second inverter the output pulse width is from 300 ps to 2 ns. The SET pulse is wider when first inverter is struck because the initial pulse is further stretched during propagation through the second inverter. When more than 12 PSCs are connected in parallel, the SETs in the second inverter cannot be detected. As depicted in Figure 6.24, for 12 PSCs the sensitivity of second inverter significantly decreases for LET < 5 MeVcm²mg⁻¹. These

results indicate that the parallel connection of 12 PSCs per array is optimal configuration for sensing the LET variations in the range from 1 to 100 MeVcm²mg⁻¹. However, it is important to note than smaller number of PSC can be chosen as well.

Based on the results depicted in Figure 6.23 and Figure 6.24, the SETs induced in a 12-cell array can be classified in two pulse width ranges, depending on whether the particle strike occurred in Inverter 1 or Inverter 2, as shown in Table 6.3. For each inverter, the SET pulses can be divided in three pulse width ranges, which correspond to the equivalent LET ranges, and denote the three criticality levels. Due to a large gap between the pulse width ranges for the two inverters of a PSC, as shown in Table 6.3, the risk of ambiguous interpretation of the SET pulse width is minimized. However, as the SET pulse width depends on the strike location, a distribution of SET pulse widths will be obtained for each LET. It is important to note that the SET pulse width variability due to strike location depends on the complexity of the circuit. In a long combinational chain in 130 nm technology, the SET pulse width may vary by more than 400 ps [115]. We expect that the pulse width distribution for PSCs would be narrow, because each PSC comprises only two sensitive transistors. However, the SET pulse width is also affected by supply voltage and temperature, as will be discussed in the following. It is therefore necessary to conduct detailed experimental or TCAD calibration in order to define a realistic SET pulse width range for a particular LET range. Hence, the number and boundaries of the SET pulse width ranges, and corresponding LET ranges, may be changed in a practical implementation.

Criticality	LET range	SET pulse width range (ns)		
level	(MeVcm ² mg ⁻¹)	Inverter 1	Inverter 2	
Low	1 - 5	4.24 - 4.46	0.24 - 0.94	
Medium	5-30	4.46 - 4.65	0.94 - 1.17	
High	30 - 100	4.65 - 4.79	1.17 - 1.30	

Table 6.3: SET pulse width ranges for a PSC in a 12-cell array

The information on the particle LET is important for accurate estimation of the combinational SER, as it defines the SET pulse width, which is linearly related to the electrical and timing masking probabilities. However, due to the stretching feature of the detector, the measured SET pulse width ranges are not the SET widths that would be induced in standard logic cells. If the standard cells are characterized as discussed in Chapter 4, the SET widths for each cell could be mapped to the equivalent SET widths for the particle detector. Table 6.4 shows the simulated SET pulse widths for three common standard cells (for low input levels), corresponding to the criticality levels defined in Table 6.3.

Criticality	SET pulse width for standard logic cells (ns)			
level	INV	NAND2	NOR2	
Low	< 0.30	< 0.28	< 0.24	
Medium	0.30 - 0.49	0.28 - 0.41	0.24 - 0.44	
High	> 0.49	> 0.41	> 0.44	

Table 6.4: SET pulse width ranges for standard cells in 130 nm library

6.4.3.3 Impact of Single Event Double Transients

To investigate the impact of Single Event Double Transients, two current pulses were simultaneously injected in different inverter pairs in the array. The obtained results were similar as in the case of serial PSC configuration, i.e. the two SET pulses eventually overlap, resulting in a single SET pulse at the output. This confirms that the parallel PSC array is also immune to multiple SETs, and would also be highly robust to erroneous SET counts.

6.4.3.4 Impact of Supply Voltage

The change of SET pulse width at the output of a 12-cell array in terms of supply voltage, when the current is successively injected in two inverters of a PSC, is shown in Figure 6.25. The illustrated results are for LET = 10 MeVcm²mg⁻¹. Similarly to the serial PSC configuration, the SET pulse width increases with the decrease of supply voltage. However, the change of SET pulse width is smaller compared to the serial configuration. It can be seen that, at the minimum investigated supply voltage of 0.8 V, the SET pulse due to strikes in Inverter 1 is wider by almost 2.8 ns compared to that for the nominal supply voltage 1.2 V, and by almost 800 ps for strikes in Inverter 2. This shows that the skew sizing enhances the pulse stretching, and voltage scaling can be leveraged for enhancing the sensitivity of PSCs to particle strikes, particularly for detection of low-LET particles. Nevertheless, minor supply voltage fluctuations, e.g. tens of mV, would cause the variation of SET pulse width in order of tens of picoseconds. This may result in erroneous classification if the SET pulse width is close to the range boundaries (see Table 6.3).

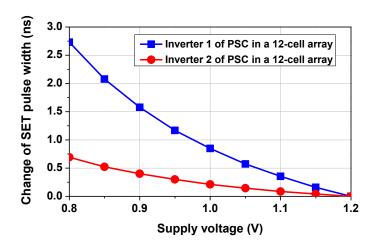


Figure 6.25: Change of SET pulse width at the output of one PSC in a 12-cell parallel array, as a function of supply voltage, for LET = $10 \text{ MeV cm}^2\text{mg}^{-1}$

6.4.3.5 Impact of Temperature

The impact of temperature variation on the SET pulse width at the output of a 12-cell array, for LET = 10 MeVcm²mg⁻¹, is illustrated in Figure 6.26. The results show the change of SET pulse width as a function of the change of temperature with respect to 27 °C, for the temperature range from -40 to 125 °C. It can be noticed that the decrease in temperature results in the decrease of the SET pulse width. For strikes in Inverter 1, the SET pulse width increases by 1.38 ns from 27 to 125 °C. On the other hand, for strikes in Inverter 2, the SET pulse width varies by less than 170 ps over the investigated temperature range. This indicates that

the skew sizing has strong impact on the temperature dependence of the PSC's SET response. The impact of temperature is particularly critical for Inverter 1, as the SET pulse width may exceed the boundaries given in Table 6.3, which could make it impossible to classify the detected SETs.

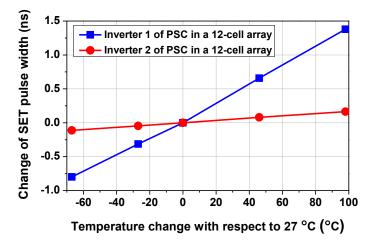


Figure 6.26: Change of SET pulse width at the output of one PSC in a 12-cell parallel array, as a function of temperature, for $LET = 10 \text{ MeV cm}^2\text{mg}^{-1}$

6.4.4 Comparison of Serial and Parallel PSC Configurations

Previous discussion has introduced detailed evaluation of the serial and parallel configurations of a particle detector based on pulse stretching inverters. From the obtained simulation results, the following features of the proposed detector configurations can be emphasized:

- Both serial and parallel PSC configurations exhibit higher sensitivity to simulated particle strikes than the standard logic cells in investigated 130 nm library. Also, both configurations can sense the SET pulses induced by very low LET (around 1 MeVcm²mg⁻¹). This qualifies both configurations as potential particle detectors.
- Serial PSC configuration offers the advantage of simpler design, as it is only required to measure the SET count rate. Using multiple short PSC chains has the advantage over long PSC chain in terms of lower latency. However, the serial connection of PSCs is not suitable for measurement of particle LET because of the SET pulse width saturation.
- Parallel PSC configuration offers the advantage of the possibility to capture both the SET count rate and the SET pulse width variations. This enables to sense the variation of the particle LET by sorting the detected SET pulses into at least three distinct pulse width ranges. Another important advantage of parallel PSC configuration is lower latency because the SET pulse has to pass only through one PSC.
- Serial PSC configuration shows stronger dependence of SET pulse width on supply voltage and temperature variations. Longer SETs at higher temperature and lower supply voltage may increase the response time, but would not affect the functionality. On the other hand, although the supply voltage and temperature variations produce smaller variations of SET pulse width in parallel

configuration, these changes may affect the accuracy of SET pulse width measurement. For this reason, in parallel configuration it is necessary to monitor the supply voltage and temperature variations and perform the online detector recalibration.

6.5 Readout Circuit Design

To construct a functional real-time radiation monitor, the particle detector should be interfaced with the appropriate readout (processing) circuitry. Considering the proposed detector designs (serial or parallel PSC configurations), two readout solutions are possible:

- *Monitoring of particle flux* by counting the SETs induced in PSCs connected in series.
- *Monitoring of particle flux and LET variations* by counting the SETs induced in PSCs connected in parallel, and binning the detected SETs according to the pulse widths.

While the simultaneous monitoring of flux and LET is generally more favorable because it provides more detailed information on the radiation environment, monitoring only the particle flux may be useful in applications where the design cost is a major constraint. Therefore, in the following discussion the possible hardware implementations of the readout circuitry for both monitoring solutions are presented. The readout solutions employ purely digital logic, which facilitates their on-chip integration.

6.5.1 Readout Circuit for Particle Flux Monitoring

For monitoring only the particle flux, the readout circuit should allow for counting the number of detected SETs in a given time period, e.g., every hour. Based on the acquired SET count rate, the average particle flux during the readout period can be determined from the experimentally obtained cross-section of the detector, using the relation (2.6) (see Section 2.4.4). As elaborated in Section 6.4, two versions of detector for SET counting are possible: (i) with a long PSC chain, and (ii) with multiple short PSC chains. The two detector implementations, and the corresponding readout circuits, are illustrated in Figures 6.27 - 6.30.

In the implementation with a single long PSC chain, illustrated in Figures 6.27 and 6.28, the output of the chain is directly interfaced to the input of processing logic. The processing logic consists of a TMR pulse counter, a register bank and a control unit. The TMR pulse counter performs the counting of detected SETs, and is designed with three 8-bit ripple counters and a majority voter. When an SET pulse is generated and propagated through the PSC chain(s), it eventually reaches the counters and acts as a clock signal, incrementing the counter state. The counter state is periodically read and stored in the register bank. The control logic is responsible for periodic reading and resetting of counters, storing the SET count in the register bank, and communication with the external logic. The size and structure of the register is sufficient for storing the number of detected SET in each hour.

In the version with multiple PSC chains, depicted in Figures 6.29 and 6.30, the sensing part is composed of N chains and each chain contains M cascaded PSCs. The outputs of all chains are connected to the OR-tree to obtain a single output, which is wired to the processing logic. Thus, a particle strike in any PSC will be manifested as a single SET pulse at the output. Two OR-tree units are employed to detect any SETs induced in the OR gates, which could result in erroneous SET count. One OR-tree is interfaced to the TMR

counter while the other is interfaced to the control unit. If an SET occurs in the detector, it will propagate through both OR trees and the counter state will be incremented, while the control unit will receive a notification of detected SET. However, if an SET occurs in one of the OR-trees, the mismatch between the counter state and the notification status in the control unit will indicate that the SET is not coming from the detector. The rest of the processing logic is the same as in the case of a long PSC chain. In comparison with the configuration based on a long PSC chain, the main advantage of the design with multiple chains is faster response, particularly if the chains consist of a small number of PSCs (e.g., up to ten PSCs).

An important design requirement for both implementations is to have as large sensing area as possible, whereby the sensing area should be significantly larger than the processing area in order to maximize the probability of particle detection. However, if the detector has to be implemented in a target chip, its area will be constrained by the available area on the chip. The TMR counter, register bank and control logic have fixed area which is independent of the sensing area. In the case of implementation with a single PSC chain, the total sensing area is defined by the total number of PSCs. Therefore, to achieve sufficiently large sensing area, the detection chain should be as long as possible. On the other hand, increasing the chain length results in a linear increase of the SET pulse width, and therefore in higher latency. Thus, using large detection area would be acceptable only if the response time is not critical. In the configuration with multiple PSCs chains, the total sensing area is defined by the number of PSCs per chain N and the total number of chains M. It is important to note that in this case the area of the OR-tree depends on the number of inverter chains. In order to reduce the area of OR-tree, and further minimize the possibility of SET occurrence in OR-trees, the 4-input OR gates with the minimum size are selected. Taking as example N =1024 (chains) and M = 20 (PSCs), and given that the area of one PSC with the previously defined sizes is around 10 μ m², the total sensing area is around 204800 μ m². For such a configuration, 341 OR4 gates, with the total area of around 4000 μ m², are required. Therefore, it can be roughly estimated that the sensing area would account for more than 85 % of the total design area, thus ensuring high sensitivity. It is important to recall than in the configuration with multiple PSC chains the detection latency is only affected by the number of PSCs per chain, and not by the number of chains. This offers greater design flexibility compared to the design with a single chain.

Both detector implementations require relatively simple processing resources. As a result, the overall implementation cost would be relatively low. Moreover, as the operating principle of the proposed detector is based on counting the transient events (SETs), and due to its inherent immunity to double SETs, the possibility of error accumulation is eliminated as long as the counters in the processing logic are periodically reset. The proposed solution also provides relatively low detection latency. In the serial PSC configuration the detection latency is in the order of ns when multiple chains are used, and in the order of μ s when a single long PSC chain is used. Another important characteristic of the presented solution is the low dynamic power consumption, since the logic level switching in the detector and processing logic occurs only when an SET is generated. We estimate that the total power consumption of the detector and processing logic would be linearly dependent on the particle count rate. To achieve sufficient radiation hardness of the readout circuit and minimize the number of erroneous counts, the radiation-hardening-by-design methods should be applied to the control unit and register file. It is important to note that the proposed readout circuit designs are generic. Depending on application requirements and design constraints, the readout circuits can be modified without affecting their basic functionality.

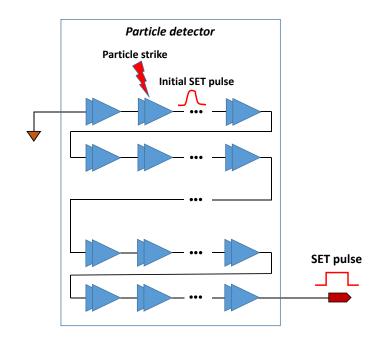


Figure 6.27: Particle detector based on a long PSC chain

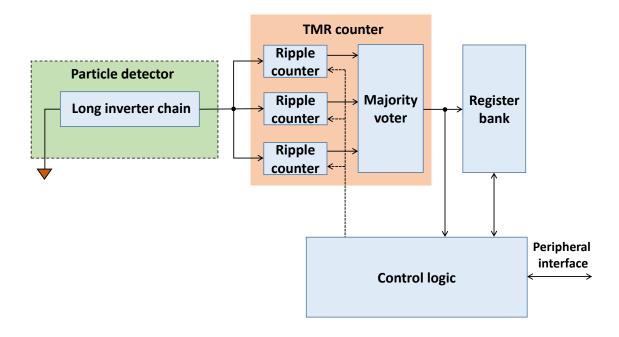


Figure 6.28: Readout circuit for particle detector based on a long PSC chain

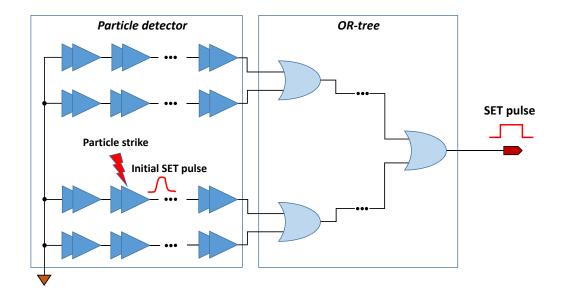


Figure 6.29: Particle detector based on multiple short PSC chains

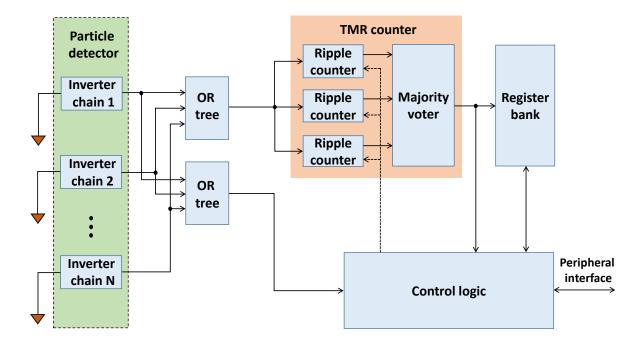


Figure 6.30: Readout circuit for particle detector based on multiple short PSC chains

6.5.2 Readout Circuit for Particle Flux and LET Monitoring

For monitoring both the particle flux and LET variation, the parallel PSC configuration is the recommended option. To achieve sufficiently large detection area, a number of PSC arrays need to be connected in parallel. The number of required arrays is determined according to the design requirements. The structure of the detector with parallel PSC configuration is illustrated in Figure 6.31, and the block diagram of the readout circuit is shown in Figure 6.32. The readout circuit performs two main tasks: (i) counting of detected SETs, and (ii) sorting of detected SETs into pulse width ranges. It is composed of four main elements: (i) OR-tree which accepts the SET pulses from the pulse stretching arrays and provides a single output pulse for further processing, (ii) two readout channels for filtering the SETs according to their width, and counting the SETs for each pulse width range, (iii) control unit for managing the operation of all blocks, and (iv) register bank for storing the measured results. Similarly to the processing logic for serial PSC configuration, an important advantage of the parallel configuration is the low power consumption, since the logic level switching in detector, OR-tree, filters and counters occurs only upon a particle strike.

The SET pulses generated at the outputs of pulse stretching arrays ($OUT_1 - OUT_M$) are propagated through the OR-tree, and the output of OR-tree is connected to the inputs of all SET filters. The OR-tree is designed as a symmetrical circuit with the same number of OR gates from all inputs to the output. The SPICE simulations have shown that positive SET pulse are broadened while propagating through the OR paths, while negative SET pulses propagate with minor attenuation or without attenuation. To minimize the propagation-induced SET pulse broadening, the SETs form the detector are inverted so that the negative pulses are propagated, and then the output of OR-tree is again inverted to restore original positive polarity. The size of the OR-tree is chosen according to the number of arrays, and in general the number of OR gates is less than 10 % of the number of PSCs. On the other hand, the number of PSC arrays is defined by the required sensing area for the target application. This is an important feature, because the detector scalability allows easier adaption to the application requirements.

Since the SET pulses induced in PCS arrays can be sorted in two pulse width ranges, depending on whether Inverter 1 or Inverter 2 is hit (see Table 6.3), the SET filters and counters are divided in two readout channels, denoted as *Readout channel 1* and *Readout channel 2*. Each readout channel is composed of K SET filters and K counters. The SET filters are implemented with custom-designed delay elements and guard gates. Each filter passes the SET pulses longer than the predefined delay, where the delays are chosen to match the boundaries of SET pulse width ranges defined in Table 6.3. Thus, for N pulse width ranges, K = N + 1. This means that "SET filter 1" has smallest delay, while "SET filter K" has largest delay. In other words, the "SET filter 1" will propagate all detected SETs, while the "SET filter K" will propagate only the longest SETs. The output of each filter is connected to a corresponding 8-bit ripple counter, which captures the number of SETs that have passed through the filter. Therefore, to obtain the right SET count for each LET range in Table 6.3, the readings of adjacent counters should be subtracted. For example, the reading of "Counter 2" has to be subtracted from the reading of "Counter 1" to obtain the SET count for the first LET range (low criticality level). The SET counts of equivalent LET ranges from the two readout channels are then summed to get the total number of counts. Thus, for a given measurement period, three values will be acquired by the readout circuit, where each value represents the number of detected SETs for one of the three LET ranges. However, in order to take into account the variability of SET pulse width, it may be needed to increase the number of ranges and counters.

The functionality of the PSC arrays, OR-tree and readout channel was verified with SPICE simulations. For the investigated operating conditions, the detection latency (time required for an SET pulse to traverse from the strike node to the counter) is in the order of several ns. This response time is significantly lower compared to the serial PSC configuration where the response can be hundreds of ns due to the pulse stretching through a longer chain.

In order to achieve high immunity of processing logic to soft errors, the radiation-hardening-by-design measures have to be applied. For sequential elements in control unit, register bank and SET counter, the triple modular redundancy is used. For combinational logic the most sensitive is the OR-tree. In the current version, the use of OR gates with driving strength x2 ensures that the SETs induced in OR-tree are shorter than the SETs in PSCs, and thus cannot be captured by the counter.

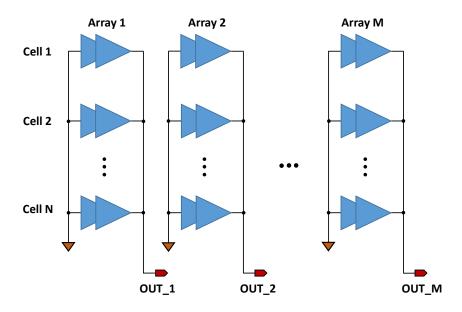


Figure 6.31: Particle detector based on PSCs connected in parallel

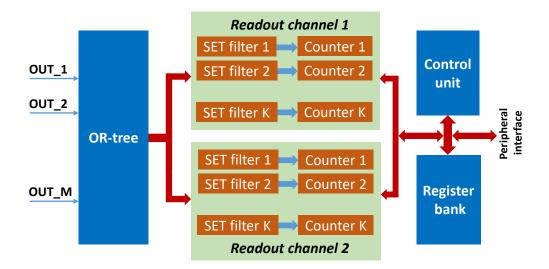


Figure 6.32: Readout circuit for particle detector based on PSCs connected in parallel

6.6 Comparison with the State-of-the-Art Particle Detectors

As elaborated in Section 3.5, various semiconductor particle detectors can be employed for monitoring of particle flux and/or LET in radiation environment. In order to evaluate the proposed particle detector against the state-of-the-art solutions, we have compared our findings with the published results for five existing detectors: bulk built-in current detectors, acoustic wave detectors, diode detectors, SRAM-based detectors, and 3D NAND flash detectors. For comparison, the proposed solution with parallel PSC configuration is considered. The comparison was performed in terms of six metrics [MA3, MA18]: (i) probability of false alarms, (ii) probability of multiple errors, (iii) detection latency, (iv) area overhead, (v) power overhead, and (vi) capability to monitor LET. The comparative analysis is summarized in Table 6.5. It is important to note that in contrast to the proposed detector and the acoustic wave detector, all other detectors have been validated through irradiation experiments. Nevertheless, the analysis is based on design and performance metrics which provide a reasonable and fair comparison.

Type of detector	Probability of false alarms	Probability of multiple errors	Detection latency	Area overhead	Power overhead	Ability to monitor LET
Built-in current detectors [262 – 268]	Moderate	Low	< 10 clock cycles	< 30 %	< 50 %	No
Acoustic wave detectors [270]	Moderate	Low	30 – 100 clock cycles	< 10 %	< 10 %	No
Diode detectors [271 – 273]	Low	Low	100s of clock cycles	> 100 %	> 100 %	Yes
SRAM detectors [274 - 277]	Low	High	> 1000 clock cycles	> 50 %	> 20 %	No (with standard SRAM)
3D NAND flash detectors [280]	Low	Low	100s of clock cycles	> 50 %	> 30 %	Yes
Pulse stretching detector	Low	Low	< 10 clock cycles	< 20 %	< 10 %	Yes

Table 6.5: Comparison of proposed particle detector with existing solutions

As previously discussed, the proposed concept of particle detection by sensing the SETs is inherently immune to multiple errors and error accumulation, because of the transient nature of SETs. This is an advantage over SRAM detectors which are sensitive to multi-bit upsets, particularly at high LET values. Unlike the bulk built-in current detectors, the proposed pulse stretching detector does not require to be connected directly to the target circuit, and hence there is low probability that the noise generated in the target system will propagate to the detector and cause false alarms. Similarly, the acoustic wave detectors

may be also prone to false alarms since the acoustic waves may be generated from sources other than the energetic particles.

The low complexity of processing logic (i.e., purely digital readout) and low area and power overhead (compared to the target system) are the main advantages of the proposed detector over diode, SRAM and 3D NAND flash detectors. As a result, integration of the proposed detector in a target chip would be easier and cheaper. To assess the area and power overhead, we have considered that all detectors have the same sensing area, and thus the key difference is in the readout logic. Because of complex mixed-signal readout circuitry, the diode detectors may typically induce the area and power overhead over 100 %. The 3D NAND flash and SRAM detectors also incur high area and power overhead due to complex readout logic. The bulk built-in current detectors and acoustic wave detectors are distributed across the target chip, enabling to detect the strike location, but this increases the overall design complexity.

Furthermore, the low detection latency of only several clock cycles (several ns) is another important advantage of the proposed detector, as most alternative solutions have slower response. For example, the SRAM-based detectors may have the response time in the order of ms due to periodic scrubbing and error detection and correction, which may take thousands of clock cycles depending on the SRAM size. Similarly, the diode and 3D NAND flash detectors also have slower response, typically in the order of hundreds of clock cycles, due to mixed-signal processing and analog-to-digital conversion.

The possibility of monitoring the LET variation stands out as the major advantage of the proposed detector over current, acoustic wave and SRAM detectors. Apart from the aforementioned advantages, it is noteworthy to mention that the main drawback of the proposed solution, in comparison to detectors which employ analog processing such as diode and 3D NAND flash detectors, is the inability to provide a fine-grained measurement of LET, because of the limited resolution of current digital readout circuit design. Nevertheless, the information on the SET count rate and the classification of SET pulse widths into several ranges are sufficient for the targeted self-adaptive processing systems.

6.7 Application in a Self-Adaptive Multi-Processor System

The proposed particle detector is intended to serve as an on-chip enabler of fault-tolerant mechanisms in a self-adaptive multi-processing system for space applications. However, it can also be realized as a standalone chip and used to trigger the fault-tolerant mechanisms in multiple chips within a complex system. The multi-processing architectures are gaining more and more interest in the context of space applications, due to their intrinsic hardware redundancy that can be leveraged to implement dynamic fault-tolerance at minimum cost. Namely, by arranging the cores into various NMR configurations, different levels of fault-tolerance can be achieved, with minimal area and power overhead related to additional logic for selecting the fault-tolerant modes. The use of particle detector, in conjunction with other on-chip sensors for monitoring the parameters influencing the system SER (e.g., temperature, supply voltage, clock frequency and aging), enables to select an optimal fault-tolerant solution under given radiation conditions and application requirements. Consequently, a trade-off between fault-tolerance, power consumption and performance can be maintained in real time. Although both proposed detector configurations (serial and parallel) can be employed in self-adaptive multi-processing systems, in this case we will consider only the parallel PSC configuration because it supports the monitoring of both particle flux and LET. A generic model of a self-adaptive multi-processing system is illustrated in Figure 6.33. Besides the processing cores, the system consists of a number of embedded sensors for status monitoring, a module for SER computation (and possibly even SER prediction), and a module for dynamic selection of operating and fault-tolerant modes. For dynamic switching of operating modes, the *Waterbear* framework controller proposed by Simevski *et al.* [58] can be employed. Based on the measured radiation levels and the application requirements, the framework controller can configure the cores into three main operating modes:

- **High performance mode**: the multiprocessor operates as a common multiprocessor, i.e., each core executes its own task.
- **Destress (or low-power) mode**: one or more cores are operating while the others are clocked- or powered-off to reduce aging and power consumption. For this purpose, dedicated aging sensors are embedded in each core.
- **Fault-tolerant mode**: based on the required level of radiation-hardness and the radiation intensity measured with the particle detector, the fault tolerance of the system can be controlled by adjusting the operating parameters (supply voltage and clock frequency), and coupling the processing cores into various NMR configurations.

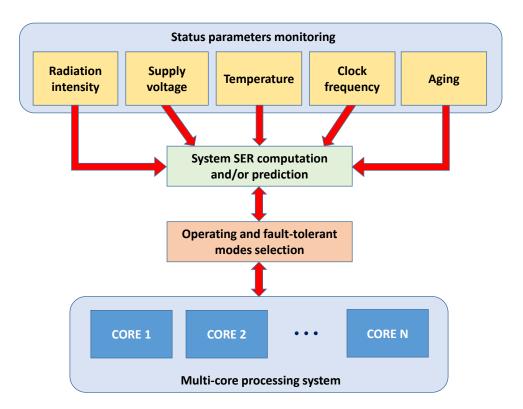


Figure 6.33: A concept of a self-adaptive microprocessor platform with online SER monitoring

During operation under radiation exposure in space, the particle detector measures the SET count rate and the SET pulse width, and classifies the measured data as explained in Section 6.5.2. Based on this information, the particle flux and LET variation can be monitored, and the variation of system SER can be tracked in real time. Although the proposed detector cannot measure actual LET of detected particles, the SET count rate and the classification of detected SETs into distinct pulse width ranges are sufficient for estimating the criticality of radiation exposure for a target system. Subsequently, the operating modes and fault-tolerant mechanisms can be adjusted during the runtime to achieve the optimal fault tolerance. A variety of core-level fault-tolerant techniques can be deployed, where the most common solutions are: supply voltage and frequency scaling, Dual Modular Redundancy (DMR), Triple Modular Redundancy (TMR), and Quadruple Modular Redundancy (QMR).

In order to compute accurately the system SER, it is necessary to establish a correlation between the response of on-chip sensors and the core-level SER. Assuming that all cores are identical, the SER will be the same for all of them under identical workload, and the sum of core-level SERs gives the total system SER. In practice, the operating mode of each core is changing during the runtime, leading to variation of the system SER. As the design and technology parameters are constant for a given system, the overall SER for a particular operating mode (task) will depend on irradiation parameters (particle flux and LET), operating parameters (supply voltage, temperature and clock frequency), total sensitive area (defined by the number of sensitive transistor under given operating mode), and aging. By characterizing the target system, either with simulations or irradiation experiments, the system SER for different operating modes and all combinations of contributing parameters can be obtained and stored in look-up tables. Based on the readings from all sensors and the data stored in look-up tables, the SER variation can be computed in real time, and appropriate fault-tolerant mechanisms can be activated by the framework controller.

Besides the real-time SER monitoring, the information obtained with the particle detector can be utilized for the prediction of SER variations. The SER prediction is essential for forecasting the onset of SPEs, allowing timely activation of fault-tolerant mechanisms. A machine learning algorithm proposed in our previous work [295] supports the prediction of SER increase at least one hour in advance, based on the measured particle count rate and previous SPE history data obtained from publicly available databases. In order to implement the machine learning prediction algorithm, a dedicated hardware accelerator is required, and one possible solution is proposed in [296]. The prediction algorithm can be upgraded to include the information on LET variation, and thus provide more accurate SER prediction.

6.8 Summary

In this chapter, an approach for online particle detection with the custom-sized pulse stretching inverters is presented. The simulation results have shown that the proposed solution could detect both the SET count rate and the SET pulse width variation, allowing to determine the particle flux and the LET variation. The proposed solution offers a cost-effective alternative over detectors that require analog processing, with a unique advantage of fully digital readout. As this work presents the initial simulation results, further work needs to be conducted to verify the functionality of the proposed solution under real radiation conditions. In that regard, the future work will be done along the following directions:

• Chip implementation of particle monitor: To evaluate the functionality of the proposed detector, both variants (with PSCs connected in series and in parallel) have to be first implemented on a chip as standalone solutions. This will initially be done for the 130 nm technology considered in this work. It is first necessary to integrate a single PSC with different sizes in the standard cell library. Then, the serial and parallel PSC configurations and associated readout electronics have to be

implemented on test chips. In order to avoid charge sharing effects, which could compromise the detector's sensitivity, special attention should be paid to layout design.

- Testing under irradiation: Conducting irradiation tests with heavy ion beams is essential for calibrating the proposed particle monitor. The main objective will be to obtain the cross-section of the detector designed in 130 nm technology, and evaluate the dependence of SET count rate and SET pulse width on the particle flux and LET. In addition, the impact of operating parameters (supply voltage and temperature) on detector's sensitivity will be evaluated. The standard heavy ion cocktails covering the LET from 1 to 100 MeVcm²mg⁻¹ will be utilized. Experimental results will enable to determine the optimum transistor sizing for a single PSC and the number of PSCs for serial/parallel configurations for achieving sufficient radiation sensitivity, as well as to establish the calibration models.
- Verification for scaled technologies: For practical application of the proposed particle monitor it is important to verify its functionality in scaled (sub-100 nm) technologies. In that regard, the characterization of a single PSC and parallel/serial PSC configurations with simulations, as well as the irradiation testing, will be done for the selected scaled technology.

Chapter 7

Conclusion

The Single Event Transients (SETs) represent a serious reliability threat for nanoscale ICs employed in harsh environments such as space, but also in safety-critical terrestrial applications. Due to the technology scaling and growing complexity of ICs on one side, and the analog nature of SET effects on the other side, the characterization, modeling and mitigation of SETs in digital designs is a challenging task. The particular challenge lies in the need to address the SET effects in combinational circuits designed with the standard logic cells that are inherently sensitive to SETs, using the standard design tools which do not have built-in support for the analysis of radiation effects. Despite significant advancement that has been achieved over the past several decades, the characterization, modeling and mitigation of SET effects in standard-cell-based designs still faces the shortcomings in terms of characterization effectiveness, model accuracy, and efficiency of the mitigation measures. In that regard, this thesis has provided a contribution to the current state-of-the-art by addressing the three important aspects of the soft-error-aware IC design: (i) characterization and modeling of SET effects in standard cell library, (ii) mitigation of SET effects in standard cells, and (iii) online particle detection as a support for dynamic fault tolerance.

7.1 Achieved Results

To facilitate the characterization and mitigation of SET effects in combinational logic, we have introduced a holistic characterization methodology, which addresses the SET effects in both the standard cells and their hardened configurations. This approach provides significant advancement over the existing characterization methodologies focused only on characterization of SET effects in standard cells, without considering the possible gate-level hardening solutions. In existing approaches, the gate-level hardening solutions are evaluated during the analysis of a particular design, which requires additional simulation effort even if the standard cell library has been already characterized. By performing the full characterization of a given standard library, in order to quantify the SET sensitivities of individual standard cells and their hardened configurations, the obtained SET database can be used a guide in choosing the optimal design solutions without the need to perform exhaustive simulations for every node in a target design.

The proposed characterization approach employs two existing current models for SET simulations, offering the flexibility and improved accuracy over the approaches using a single bias-independent current

model. For the most common combinational cells, the SET sensitivity was quantified in terms of critical charge, generated SET pulse width and propagated SET pulse width, for different design and operating parameters. The results have confirmed differing SET sensitivity of standard cells, as well as differing contribution of design and operating parameters to the SET sensitivity. To the best of our knowledge, the impact of SETs on standard delay cells has been studied for the first time, and it has been shown that these cells are the most sensitive due to the skew sizing.

Using the characterization results, the fitting models for critical charge, generated SET pulse width and propagated SET pulse width, in terms of analyzed design and operating parameters, have been derived. All proposed models have a relative error less than 10 % compared to SPICE simulations, for most analyzed test cases. Analytical models can be used to predict in the early design phases the SET sensitivity of individual logic cells and their contribution to the total SER. The proposed models employ the principle of superposition, thus allowing to differentiate the impact of various contributing factors on the SET sensitivity of a target gate. As a result, the operating conditions (supply voltage, temperature and input logic levels) for achieving the best SET robustness can be estimated. Moreover, the derived models express the SET sensitivity of standard cells in terms of relevant design parameters, thus ensuring that all technological aspects and design details (e.g. internal structure of logic cells) remain transparent to the designer. This is an essential improvement over existing SET sensitivity models which require the knowledge of transistor sizes or proprietary technological parameters.

Besides the benefit of joint characterization of standard logic cells and respective gate-level hardening configurations, the proposed methodology allows for reducing both the total number of simulations during characterization and the amount of data in the output SET database for the target library. Exploiting the inherent similarities in the SET response of multi-input gates for different input logic levels, the number of required simulation runs for characterizing the three- and four-input standard cells can be reduced by almost 50 %. Furthermore, in contrast to standard approaches where the raw simulation data is stored in LUTs, our approach is based on storing the coefficients of derived SET sensitivity models in LUTs instead of raw data. As a result, the overall amount of characterization data can be reduced by more than two orders of magnitude, enabling more time-efficient subsequent SER analysis.

For the purpose of gate-level SET mitigation in standard combinational cells, we have proposed for the first time the use of decoupling cells, which are originally employed for filtering the power supply noise. By inserting two decoupling cells at the output of a logic gate, the critical charge of the gate's output node is increased and its capability to filter the incoming SETs is improved. The particular benefit is that the decoupling cells are highly robust to direct particle strikes. We have performed detailed characterization of the proposed technique and seven existing techniques, in order to quantify their contribution to the SET robustness improvement of individual logic gates and the resulting area, delay and power overhead. It was shown that the proposed technique based on decoupling cells provides better SET filtering than the two most common gate-level techniques (gate upsizing and gate duplication), and also better performance in terms of SET generation than several alternative techniques. However, all investigated techniques exhibit complementary advantages. As a result, a particular technique may be affective for improving the SET robustness of one type of gate, but less effective for another type of gate. Based on these observations, a set of recommendations for the application of each technique has been defined, which can be used as a guide-

line for combined application of multiple techniques. Applying two or three hardening techniques provides a better SET-suppression than applying a single technique, which has been verified on the example of a random combinational chain.

To allow for efficient and cost-effective online monitoring of energetic particles, as a support for the dynamic activation of system-level fault tolerance, we have proposed for the first time a particle detector based on custom-sized pulse stretching inverter chains. The proposed solution is primarily intended for the on-chip integration in self-adaptive fault-tolerant systems for space missions. Measuring the radiation levels in real time enables the autonomous triggering of the fault-tolerant mechanisms under high radiation levels, or alternatively the shutting down of sensitive units to avoid the radiation-induced damage. The operating principle is based on counting the detected SETs to determine the particle flux, and sensing the variation of the SET pulse width to track the LET variations. Due to the unique skew sizing, the induced SET pulses are stretched after propagating through a single stage, which facilitates the detection of low-LET particles (below 1 MeVcm²mg⁻¹). The SPICE simulations have shown that the LET variation from 1 to 100 MeVcm²mg⁻¹ causes the variation of SET pulse width at the detector's output by approximately 550 ps. In comparison to the state-of-the-art, our approach is a step ahead regarding the three main requirements of space-borne self-adaptive systems: (i) possibility to monitor both LET and particle flux providing detailed information on the radiation conditions, (ii) low energy consumption and detection latency secured by lowcomplexity digital processing logic, and (iii) immunity to false alarms and error accumulation due to the transient nature of detected SETs.

The results of this work can be leveraged as a basis for establishing a comprehensive multi-level radhard design flow. To the best of our knowledge, there is currently no any industrial solution for multi-level rad-hard design flow for ICs based on standard cell libraries, which supports both the characterization and mitigation of soft errors, as well as the design of online soft error monitoring. Introducing such solutions into standard IC design tools is essential for the design of soft-error-aware ICs for applications featuring variable radiation conditions, primarily for space missions. To obtain a widely applicable solution, the multi-level rad-hard design flow needs to be flexible in the sense that the evaluation and hardening techniques can be customized to a particular design. Addressing the radiation effects in standard cells is also important from the perspective of future space missions oriented towards low-cost satellites, where the use of standard cells is more cost-effective than the custom design of rad-hard cells.

7.2 Future Work

Although the results presented in this thesis have addressed the objectives outlined in Chapter 1, further work may be focused on incorporation of the proposed solutions into a multi-level rad-hard design flow that can be applied in the design of soft-error-aware ICs. This section briefly summarizes the key strategic directions of future work.

The follow-up work on characterization and modeling of SET effects can be performed along two main directions: (i) increasing the accuracy of characterization and modeling, (ii) integration of the SET database for standard cell library into an overall SER analysis framework. The SET characterization methodology and the SET sensitivity models need to be extended by including the effects which are relevant for advanced

technologies. In that context, the process variations, manufacturing detects, aging and crosstalk need to be considered. Furthermore, the cell positioning in the layout and details of radiation-matter interaction are essential for considering the charge sharing effects which cause the SEMTs. Although the aforementioned effects have been widely explored, there is still no a comprehensive approach for joint characterization of all relevant effects in standard cells. By increasing the number of effects considered in the characterization, the resulting SET database will essentially be turned into a complex multidimensional space, and thus it would become more difficult or even impossible to establish the fitting-based SET models. A possible solution could be the modeling based on machine learning algorithms, which are especially suitable for analysis of multi-dimensional space datasets. Further effort has to be invested into integration of the proposed characterization and mitigation solutions into a SER analysis flow which addresses both SETs and SEUs. It is important to abstract the electrical characterization results from SPICE simulations in order to enable their usage at circuit and system levels. Various approaches can be considered such as the use of neural networks, structural circuit analysis and circuit partitioning.

In order to enable the cost-effective gate-level SET mitigation, it is important to establish an approach for selection of the optimal combination of gate-level mitigation techniques for an arbitrary design. Such approach needs to ensure that the hardening solutions are applied to a minimum set of the most sensitive gates, providing maximum reduction of SER with minimum area, delay and power overhead. The basis for the combined application of multiple techniques could be the recommendations outlined in Chapter 5. In that regard, the use of multiple gate-level hardening techniques needs verification on complex designs. A particular challenge will be in optimizing the application of gate-level approaches in combination with the techniques used at the circuit/RTL level such as supply voltage and frequency scaling, gate placement, error detection and correction, etc.

Regarding the particle detection with pulse stretching inverters, along with the necessity to validate the concept under irradiation, the key direction for future work is to enable the seamless integration of particle detector in a real self-adaptive fault-tolerant system. In that regard, it is important to address two aspects. First, as the system SER depends on multiple parameters (radiation exposure, supply voltage, temperature, clock frequency, aging), it is essential to sense all these parameters collaboratively in order to enable accurate tracking of SER variations. Second, the hardware for processing the information from the detector and calculating the SER of a target system in real time has to be designed. The major challenge in this case is to customize the design of particle detector to the application requirements, since the detector area is constrained by the total available area on the target chip. In that context it is particularly important to investigate how the limitations in the sensing area affect the overall sensitivity of the detector, and how the on-chip positioning of the detector affects its performance.

Successful accomplishment of proposed future research tasks, together with the achieved results in this work, would be useful for establishing a rad-hard design approach for standard cell libraries, and can also serve as a basis for design of resilient self-aware ICs.

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